



U74CBTLV3125

CMOS IC

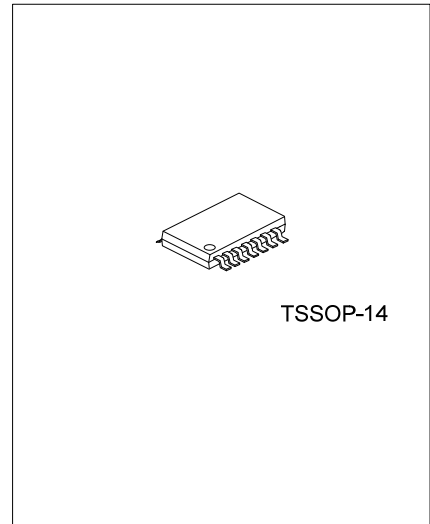
LOW-VOLTAGE QUADRUPLE FET BUS SWITCH

DESCRIPTION

The **U74CBTLV3125** quadruple FET bus switch features independent line switches. Each switch is disabled when the associated output-enable (\overline{OE}) input is high.

The device is fully specified for partial-power-down applications using I_{off} . The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.



TSSOP-14

FEATURES

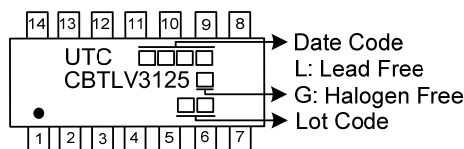
- * 5-Ω Switch Connection Between Two Ports
- * Standard '125-Type Pinout
- * Isolation Under Power-Off Conditions

ORDERING INFORMATION

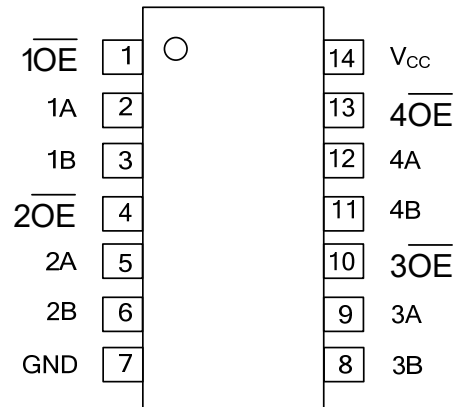
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74CBTLV3125L-P14-R	U74CBTLV3125G-P14-R	TSSOP-14	Tape Reel

<p>U74CBTLV3125G-P14-R</p> <p>(1) Packing Type (2) Package Type (3) Green Package</p>	<p>(1) R: Tape Reel (2) P14: TSSOP-14 (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING



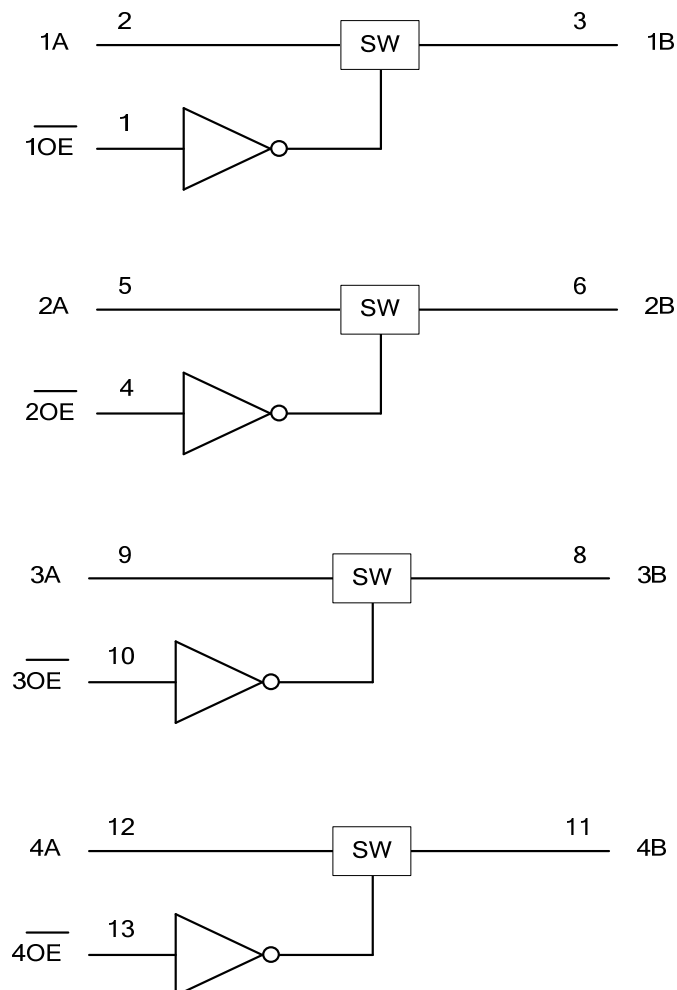
■ PIN CONFIGURATION



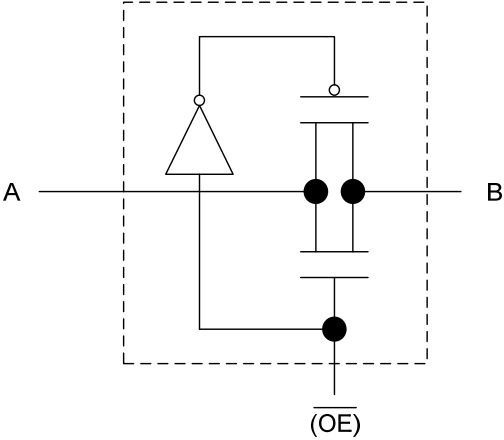
■ FUNCTION TABLE (each bus switch)

INPUT \overline{OE}	FUNCTION
L	A port = B port
H	Disconnect

■ LOGIC DIAGRAM (positive logic)



■ SIMPLIFIED SCHEMATIC (each FET switch)



■ ABSOLUTE MAXIMUM RATING (Unless otherwise specified)(Note 1)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5~4.6	V
Input Voltage	V_I	-0.5~4.6	V
Continuous channel current		128	mA
Input Clamp Current($V_{I/O}<0$)	I_{IK}	-50	mA
Storage Temperature	T_{STG}	-65 ~ +150	°C

Notes: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

■ RECOMMENDED OPERATING COMDITIONS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		2.3		3.6	V
High-control input voltage	V_{IH}	$V_{CC}=2.3V\sim 2.7V$	1.7			V
		$V_{CC}=2.7V\sim 3.6V$	2			V
Low-control input voltage	V_{IL}	$V_{CC}=2.3V\sim 2.7V$			0.7	V
		$V_{CC}=2.7V\sim 3.6V$			0.8	V
Operating Temperature	T_A		-40		+125	°C

Note: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	113	°C/W

■ STATIC CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Digital Input Diode Voltage	V_{IK}	$V_{CC}=3V, I_I=-18mA$			-1.2	V	
Input Leakage Current	I_I	$V_{CC}=3.6V, V_I=V_{CC}$ or GND			± 1	μA	
Power off Leakage Carrent	I_{off}	$V_{CC}=0, V_I$ or $V_O=0$ to 4.5V			10	μA	
Quiosceut Supply Current	I_{CC}	$V_{CC}=3.6V, V_I=V_{CC}$ or GND, $I_O=0$			10	μA	
Additional Quiescent Supply Current	ΔI_{CC}	Control Input; $V_{CC}=3.6V$, One input at 3V, Other inputs at V_{CC} or GND			300	μA	
Control input Capacitance	C_I	Control Input; $V_O=3V$ or 0		2.5		pF	
I/O Capacitance (OFF)	$C_{I/O(OFF)}$	$V_O=3V$ or 0, OE=GND		7		pF	
Resistor between two ports	R_{ON}	$V_{CC}=2.3V$ Typ. at $V_{CC}=2.5V$	$V_I=0$	$I_I=64mA$	5	8	Ω
			$V_I=1.7V$	$I_I=-15mA$	5	8	Ω
		$V_{CC}=3V$	$V_I=0V$	$I_I=64mA$	5	7	Ω
				$I_I=24mA$	5	7	Ω
			$V_I=2.4V$	$I_I=-15mA$	10	15	Ω

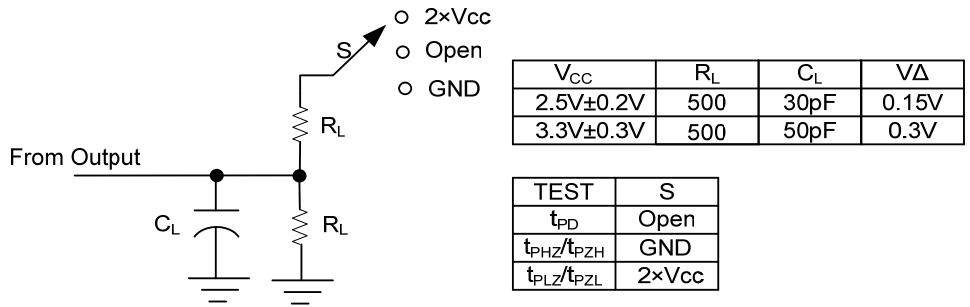
Note: All typical values are at $V_{CC}=3.3V, T_A=25^\circ C$, unless otherwise noted.

■ DYNAMIC CHARACTERISTICS (Unless otherwise specified)

See Fig. 1 and Fig. 2 for test circuit and waveforms.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
From input (A or B) to output (B or A)	t_{pd} (t_{PLH}/t_{PHL})	$V_{CC}=2.5V\pm 0.2V$			0.35	ns
		$V_{CC}=3.3V\pm 0.3V$			0.25	ns
From input (OE) to output (A or B)	t_{en} (t_{PZL}/t_{PZH})	$V_{CC}=2.5V\pm 0.2V$	2		4.6	ns
		$V_{CC}=3.3V\pm 0.3V$	2		4.4	ns
From input (OE) to output (A or B)	t_{dis} (t_{PLZ}/t_{PHZ})	$V_{CC}=2.5V\pm 0.2V$	1.1		3.9	ns
		$V_{CC}=3.3V\pm 0.3V$	1.0		4.2	ns

TEST CIRCUIT AND WAVEFORMS



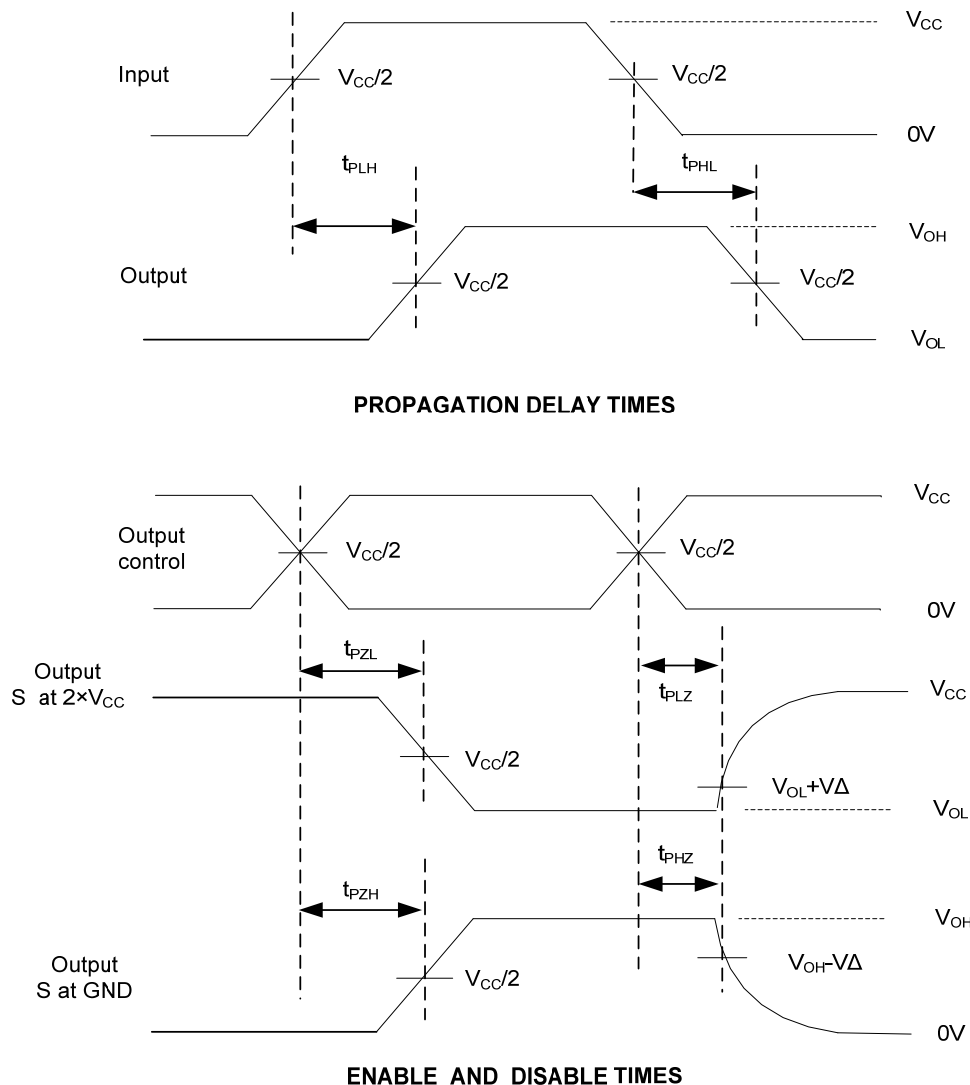
Note: C_L includes probe and jig capacitance.

t_{PLZ} and t_{PHZ} are the same as t_{dis} .

t_{PZL} and t_{PZH} are the same as t_{en} .

t_{PLH} and t_{PHL} are the same as t_{PD} .

Fig. 1 Load circuitry for switching times.



Note: All input pulses are supplied by generators having the following characteristics:

$t_r, t_f \leq 2ns$; PRR $\leq 10MHz$; $ZO=50\Omega$.

Fig. 2 Propagation delay from input(A) to output(B) and Output transition time.

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