



UNISONIC TECHNOLOGIES CO., LTD

U74CBTLV3126

CMOS IC

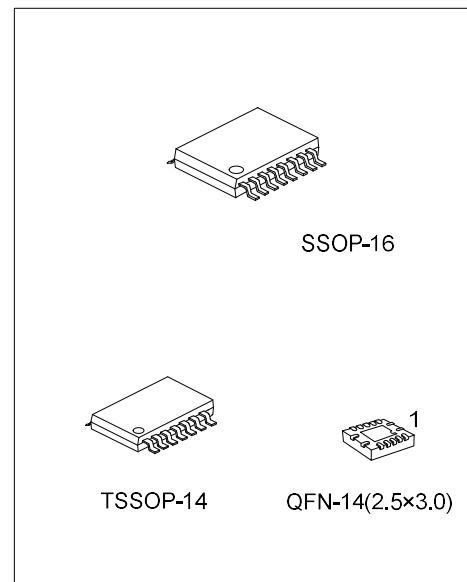
LOW-VOLTAGE QUADRUPLE FET BUS SWITCH

■ DESCRIPTION

The **U74CBTLV3126** quadruple FET bus switch features independent line switches. Each switch is disabled when the associated output-enable (OE) input is low.

The device is fully specified for partial-power-down applications using I_{off} . The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

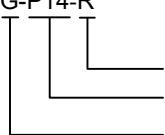


■ FEATURES

- * 5- Ω Switch Connection Between Two Ports
- * Standard '126-Type Pinout
- * I_{off} Supports Partial-Power-Down Mode Operation

■ ORDERING INFORMATION

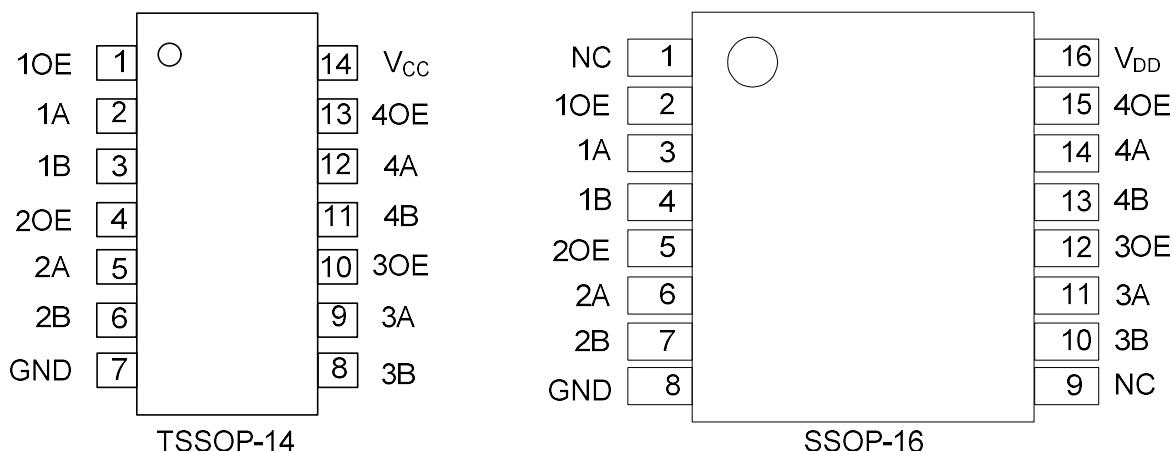
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74CBTLV3126L-P14-R	U74CBTLV3126G-P14-R	TSSOP-14	Tape Reel
U74CBTLV3126L-R16-R	U74CBTLV3126G-R16-R	SSOP-16	Tape Reel
U74CBTLV3126L-Q14-2530-R	U74CBTLV3126G-Q14-2530-R	QFN-14(2.5x3.0)	Tape Reel

U74CBTLV3126G-P14-R 	(1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) P14: TSSOP-14, R16: SSOP-16 Q14-2530: QFN-14(2.5x3.0) (3) G: Halogen Free and Lead Free, L: Lead Free
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■ MARKING

PACKAGE	MARKING
TSSOP-14	<p>The diagram shows a TSSOP-14 package with pins numbered 1 through 14. The marking area is located between pins 8 and 14. It contains the text "UTC" above "CBTLV3126". Below the text are four small squares. A dot is located to the left of the marking area. Arrows point from specific parts of the marking to the following labels:<ul style="list-style-type: none">Date Code (points to the first two squares)L: Lead Free (points to the third square)G: Halogen Free (points to the fourth square)Lot Code (points to the bottom row of pins 1-7)</p>
SSOP-16	<p>The diagram shows an SSOP-16 package with pins numbered 1 through 16. The marking area is located between pins 9 and 16. It contains the text "UTC" above "CBTLV6". Below the text are four small squares. A dot is located to the left of the marking area. Arrows point from specific parts of the marking to the following labels:<ul style="list-style-type: none">Date Code (points to the first two squares)L: Lead Free (points to the third square)G: Halogen Free (points to the fourth square)Lot Code (points to the bottom row of pins 1-8)</p>
QFN-14(2.5×3.0)	<p>The diagram shows a QFN-14 package with pins numbered 1 through 14. The marking area is located between pins 9 and 14. It contains the text "LV3126" above a small square. Arrows point from specific parts of the marking to the following labels:<ul style="list-style-type: none">L: Lead Free (points to the small square)G: Halogen Free (points to the bottom row of pins 1-7)</p>

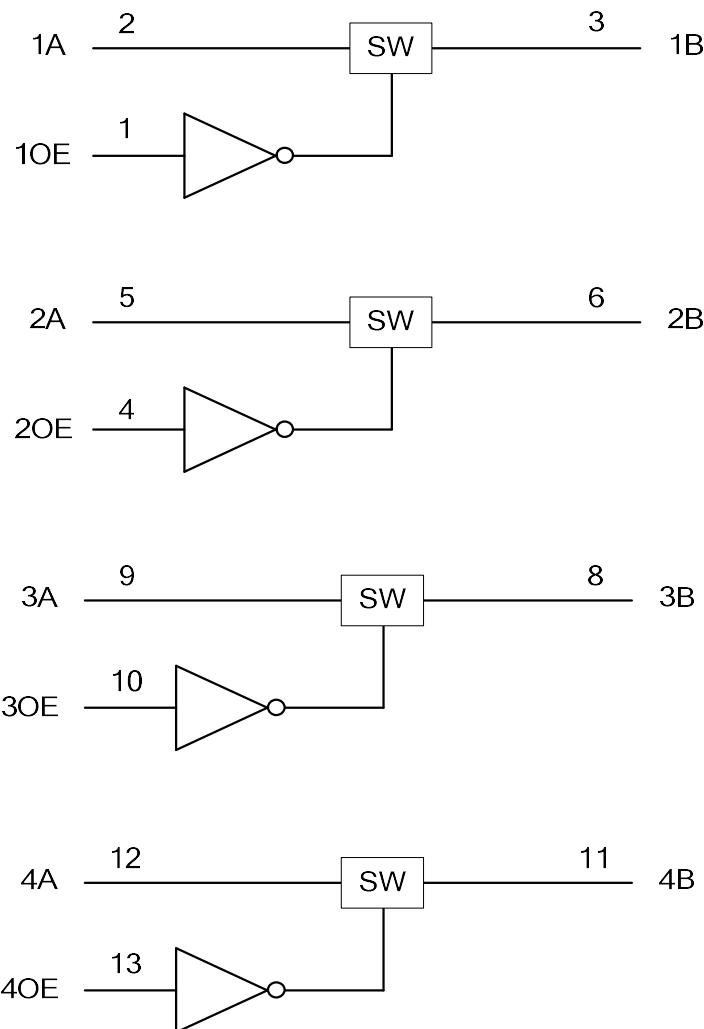
■ PIN CONFIGURATION



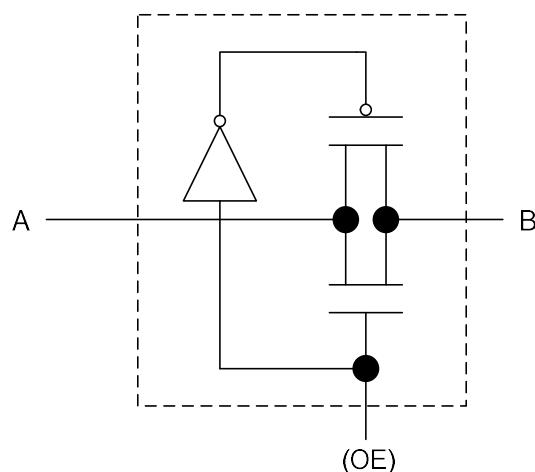
■ FUNCTION TABLE (each bus switch)

INPUT OE	FUNCTION
H	A port = B port
L	Disconnect

■ **LOGIC DIAGRAM** (positive logic)



■ **SIMPLIFIED SCHEMATIC** (each FET switch)



■ ABSOLUTE MAXIMUM RATING (unless otherwise specified)(Note 1)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V _{CC}	-0.5~4.6	V
Input Voltage	V _I	-0.5~4.6	V
Continuous channel current		128	mA
Input Clamp Current(V _{I/O} <0)	I _{IK}	-50	mA
Storage Temperature	T _{STG}	-65 ~ +150	°C

Note: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	TSSOP-14	113	°C/W
	SSOP-16	90	°C/W
	QFN-14(2.5×3.0)	104	°C/W

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V _{CC}		2.3		3.6	V
High-control input voltage	V _{IH}	V _{CC} =2.3V~2.7V	1.7			V
		V _{CC} =2.7V~3.6V	2			V
Low-control input voltage	V _{IL}	V _{CC} =2.3V~2.7V			0.7	V
		V _{CC} =2.7V~3.6V			0.8	V
Operating Temperature	T _A		-40		+125	°C

Note: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

■ STATIC CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Digital Input Diode Voltage	V _{IK}	V _{CC} =3V, I _I =-18mA			-1.2	V	
Input Leakage Current	I _I	V _{CC} =3.6V, V _i =V _{CC} or GND			±1	µA	
Power off Leakage Current	I _{OFF}	V _{CC} =0, V _I or V _O =0 to 3.6V			10	µA	
Quiescent Supply Current	I _{CC}	V _{CC} =3.6V, V _i = V _{CC} or GND, I _O =0			10	µA	
Additional Quiescent Supply Current	ΔI _{CC}	V _{CC} =3.6V, One input at 3V, Other inputs at V _{CC} or GND			300	µA	
Control input Capacitance	C _I	V _O =3V or 0		2.5		pF	
I/O Capacitance (OFF)	C _{IO(OFF)}	V _O =3V or 0, OE=GND		7		pF	
Resistor between two ports	R _{ON}	V _{CC} =2.3V TYP at V _{CC} =2.5V	I _I =0	I _I =64mA	5	8	Ω
			I _I =24mA		5	8	Ω
			I _I =1.7V	I _I =-15mA	27	40	Ω
			I _I =0V	I _I =64mA	5	7	Ω
			I _I =2.4V	I _I =24mA	5	7	Ω
				I _I =-15mA	10	15	Ω

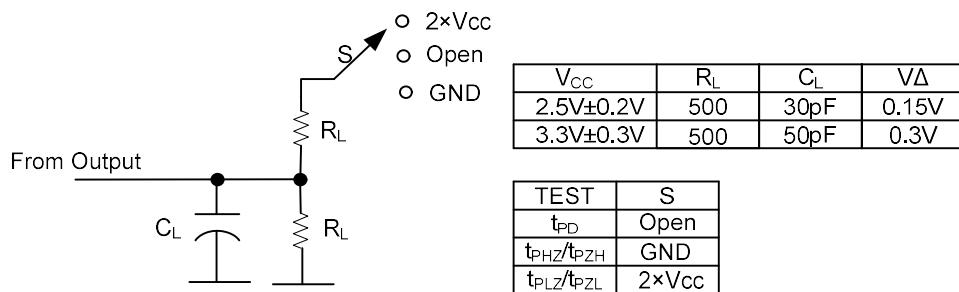
Note: All typical values are at V_{CC}=3.3V, T_A=25°C, unless otherwise noted.

■ DYNAMIC CHARACTERISTICS

See Fig. 1 and Fig. 2 for test circuit and waveforms.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
From input (A or B) to output (B or A)	t_{pd} (t_{PLH}/t_{PHL})	$V_{CC}=2.5V \pm 0.2V$			0.15	ns
		$V_{CC}=3.3V \pm 0.3V$			0.25	ns
From input (OE) to output (A or B)	t_{en} (t_{PZL}/t_{PZH})	$V_{CC}=2.5V \pm 0.2V$	1.6		4.5	ns
		$V_{CC}=3.3V \pm 0.3V$	1.9		4.2	ns
From input (OE) to output (A or B)	t_{dis} (t_{PLZ}/t_{PHZ})	$V_{CC}=2.5V \pm 0.2V$	1.3		4.7	ns
		$V_{CC}=3.3V \pm 0.3V$	1.0		4.8	ns

■ TEST CIRCUIT AND WAVEFORMS



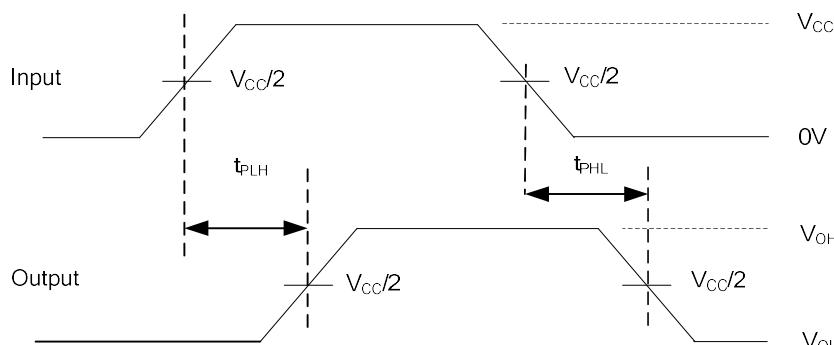
Note: C_L includes probe and jig capacitance.

t_{PLZ} and t_{PHZ} are the same as t_{dis} .

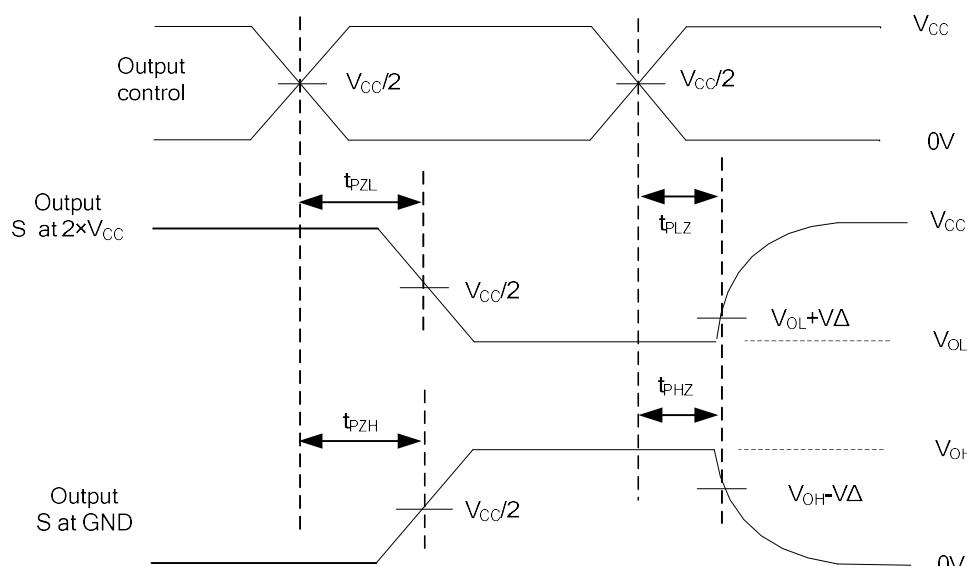
t_{PZL} and t_{PZH} are the same as t_{en} .

t_{PLH} and t_{PHL} are the same as t_{PD} .

Fig. 1 Load circuitry for switching times



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

Note: All input pulses are supplied by generators having the following characteristics:

$t_r, t_f \leq 2\text{ns}$; $P_{RR} \leq 10\text{MHz}$; $Z_0=50\Omega$.

Fig. 2 Propagation delay from input(A) to output(B) and Output transition time

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