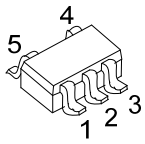
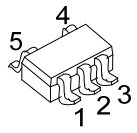
U74AUP1G06

CMOS IC

LOW-POWER SINGLE INVERTER BUFFER/DRIVER WITH OPEN-DRAIN OUTPUTS



SOT-23-5
(JEDEC TO-236)



SOT-353

X2DFN1010-6

■ DESCRIPTION

The **U74AUP1G06** is a single inverting buffer with open-drain outputs and it provides the function $Y=\overline{A}$ in positive logic. The output of this device is open-drain, and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.

This device is ensures a very low static and dynamic power consumption across the entire V_{CC} range from 0.8V to 3.6V.

This device has power-down protective circuit, preventing device destruction when it is powered down.

■ FEATURES

* Wide supply voltage range from 0.8V to 3.6V
* Inputs accept voltages up to 3.6V
* I_{OFF} supports partial-power-down mode
* Low static power consumption; I_{CC}=0.5μA (Max.)
* Optimized for 3.3V Operation

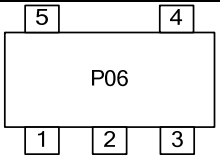
■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74AUP1G06L-AE5-R	U74AUP1G06G-AE5-R	SOT-23-5	Tape Reel
U74AUP1G06L-AL5-R	U74AUP1G06G-AL5-R	SOT-353	Tape Reel
U74AUP1G06L-K06-1010X2-R	U74AUP1G62G-K06-1010X2-R	X2DFN1010-6	Tape Reel

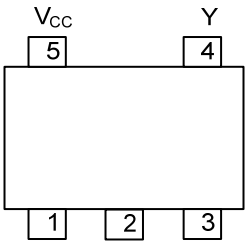
U74AUP1G06G-AE5-R
(1)Packing Type
(2)Package Type
(3)Green Package

(1) R: Tape Reel
(2) AE5: SOT-23-5, AL5: SOT-353,
K06-1010X2: X2DFN1010-6
(3) G: Halogen Free and Lead Free, L: Lead Free

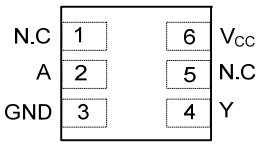
■ MARKING

SOT-23-5 / SOT-353	X2DFN1010-6
	

■ PIN CONFIGURATION



SOT-23-5 / SOT-353



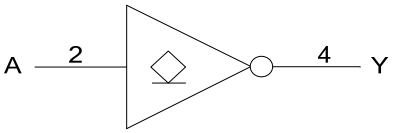
X2DFN1010-6
(TOP VIEW)

■ FUNCTION TABLE

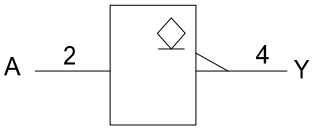
INPUT(A)	OUTPUT(Y)
H	L
L	Z

Note: H: HIGH voltage level; L: LOW voltage level; Z: high impedance state.

■ LOGIC DIAGRAM (positive logic)



Logic symbol



IEC logic symbol

■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{CC}		-0.5 ~ +4.6	V
Input Voltage	V_{IN}		-0.5 ~ +4.6	V
Output Voltage	V_{OUT}	Output in the high or low state	-0.5 ~ V_{CC} +0.5	V
		Output in the power-off state	-0.5 ~ +4.6	V
Continuous V_{CC} or GND Current	I_{CC}		±50	mA
Continuous Output Current	I_{OUT}	V_{OUT}=0 ~ V_{CC}	±20	mA
Input Clamp Current	I_{IK}	V_{IN}<0	-50	mA
Output Clamp Current	I_{OK}	V_{OUT} >V_{CC} or V_{OUT}<0	-50	mA
Storage Temperature Range	T_{STG}		-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	Operating	0.8		3.6	V
Input Voltage	V_{IN}		0		3.6	V
Output Voltage	V_{OUT}	High or low state	0		V_{CC}	V
Input Transition Rise or Fall Rate	Δt/Δv	V_{CC}=0.8V ~ 3.6V			200	ns/V
Operating Temperature	T_A		-40		+125	°C

■ ELECTRICAL CHARACTERISTICS (T_A=25°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
High-level Input Voltage	V_{IH}	V_{CC}=0.8V		V_{CC}			V
		V_{CC}=1.1V~1.95V		0.65×V_{CC}			V
		V_{CC}=2.3V~2.7V		1.6			V
		V_{CC}=3.0V~3.6V		2			V
Low-level Input Voltage	V_{IL}	V_{CC}=0.8V				0	V
		V_{CC}=1.1V~1.95V				0.35×V_{CC}	V
		V_{CC}=2.3V~2.7V				0.7	V
		V_{CC}=3.0V~3.6V				0.9	V
Low-Level Output Voltage	V_{OL}	V_{CC}=0.8V~3.6V, I_{OL}=20μA				0.1	V
		V_{CC}=1.1V, I_{OL}=1.1mA				0.3×V_{CC}	V
		V_{CC}=1.4V, I_{OL}=1.7mA				0.31	V
		V_{CC}=1.65V, I_{OL}=1.9mA				0.31	V
		V_{CC}=2.3V	I_{OL}=2.3mA			0.31	V
			I_{OL}=3.1mA			0.44	v
		V_{CC}=3.0V	I_{OL}=2.7mA			0.31	V
			I_{OL}=4.0mA			0.44	v
Input Leakage Current	$I_{I(LEAK)}$	V_{CC}=0V~3.6V, V_{IN}=GND ~ 3.6				±0.1	μA
Power OFF Leakage Current	I_{OFF}	V_{CC}=0V, V_{IN} or V_{OUT}=0V~3.6V				±0.2	μA
Additional Power OFF Leakage Current	ΔI_{OFF}	V_{CC}=0V~0.2V, V_{IN} or V_{OUT}=0V~3.6V				±0.2	μA
Quiescent Supply Current	I_{CC}	V_{CC}=0.8V~3.6V, I_{OUT}=0 V_{IN}=GND or V_{CC} ~ 3.6V				0.5	μA
Additional Quiescent Supply Current Per Input Pin	ΔI_{CC}	V_{CC}=3.3V, V_{IN}=V_{CC}-0.6V, I_{OUT}=0				40	μA
Input Capacitance	C_I	V_{CC}=0V, V_{IN}=V_{CC} or GND			1.5		pF
		V_{CC}=3.6V, V_{IN}=V_{CC} or GND			1.7		pF
Output Capacitance	C_{OUT}	V_{CC} =0V, V_{OUT}=GND			1.7		pF

■ SWITCHING CHARACTERISTICS (T_A=25°C, Input: t_R / t_F=3ns, unless otherwise specified)

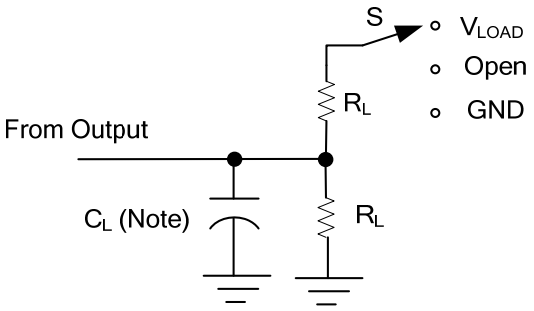
See Fig. 1 and Fig. 2 for test circuit and waveforms.

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Propagation delay from input (A) to output(Y)	t_{PD}	C_L=5pF, R_L=5kΩ	V_{CC}=0.8V		12.8		ns
			V_{CC}=1.1V±0.1V	2.3	12		ns
			V_{CC}=1.5V±0.1V	1.8	3.5		Ns
			V_{CC}=1.8V±0.15V	1.5	3.1		ns
			V_{CC}=2.5V±0.2V	1.2	2.2		ns
			V_{CC}=3.3V±0.3V	1.1	2.2		ns
		C_L=10pF, R_L=5kΩ	V_{CC}=0.8V		15.8		ns
			V_{CC}=1.1V±0.1V	2.7	12		ns
			V_{CC}=1.5V±0.1V	2.2	4.3		ns
			V_{CC}=1.8V±0.15V	1.9	3.9		ns
			V_{CC}=2.5V±0.2V	1.9	2.9		ns
			V_{CC}=3.3V±0.3V	1.6	3.0		ns
		C_L=15pF, R_L=5kΩ	V_{CC}=0.8V		18.8		ns
			V_{CC}=1.1V±0.1V	3.2	12		ns
			V_{CC}=1.5V±0.1V	2.6	5.0		ns
			V_{CC}=1.8V±0.15V	2.3	4.8		ns
			V_{CC}=2.5V±0.2V	2.1	3.5		ns
			V_{CC}=3.3V±0.3V	2.0	3.8		ns
		C_L=30pF, R_L=5kΩ	V_{CC}=0.8V		27.8		ns
			V_{CC}=1.1V±0.1V	4.4	12		ns
			V_{CC}=1.5V±0.1V	3.6	7.6		ns
			V_{CC}=1.8V±0.15V	3.2	7.4		ns
			V_{CC}=2.5V±0.2V	2.9	5.4		ns
			V_{CC}=3.3V±0.3V	2.9	6.5		ns

■ OPERATING CHARACTERISTICS (f=10MHz, T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	V_{CC}=0.8V		1.0		pF
		V_{CC}=1.1V±0.1V		1.0		pF
		V_{CC}=1.5V±0.1V		1.0		pF
		V_{CC}=1.8V±0.15V		1.0		pF
		V_{CC}=2.5V±0.2V		1.0		pF
		V_{CC}=3.3V±0.3V		1.0		pF

■ TEST CIRCUIT AND WAVEFORMS



TEST	S
t_{PZL} (Note 1)	V_{LOAD}
t_{PLZ} (Note 1)	V_{LOAD}

Note:1. Since this device has open drain outputs, the t_{PLZ} and t_{PZL} is the same as t_{PLH} and t_{PHL}.

Fig. 1 LOAD CIRCUITRY FOR SWITCHING TIMES

V_{CC}	V_{IN}	t_R / t_F	V_M	V_{LOAD}	C_L	R_L	$V_\triangle$
0.8	V_{CC}	3ns	V_{CC}/2	2×V_{CC}	5,10,15,30pF	5kΩ	0.1V
1.2±0.1V	V_{CC}	3ns	V_{CC}/2	2×V_{CC}	5,10,15,30pF	5kΩ	0.1V
1.5±0.1V	V_{CC}	3ns	V_{CC}/2	2×V_{CC}	5,10,15,30pF	5kΩ	0.1V
1.8±0.15V	V_{CC}	3ns	V_{CC}/2	2×V_{CC}	5,10,15,30pF	5kΩ	0.15V
2.5±0.2V	V_{CC}	3ns	V_{CC}/2	2×V_{CC}	5,10,15,30pF	5kΩ	0.15V
3.3±0.3V	V_{CC}	3ns	V_{CC}/2	2×V_{CC}	5,10,15,30pF	5kΩ	0.3V

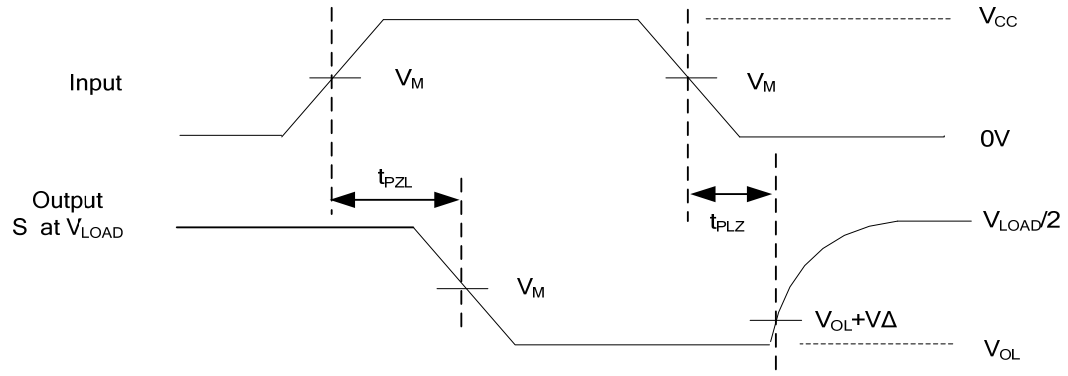


Fig. 2 PROPAGATION DELAY FROM INPUT(A) TO OUTPUT(Y) AND OUTPUT TRANSITION TIME

Notes: 1. C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: PRR ≤10MHz, Z_O = 50Ω.