



UCD4002B

Preliminary

CMOS IC

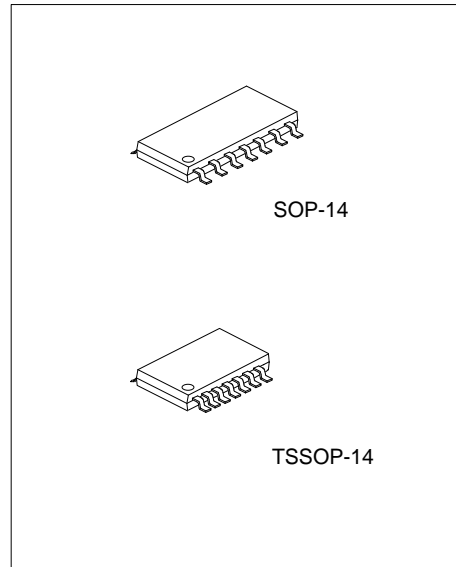
CMOS NOR GATES HIGH-VOLTAGE TYPES

DESCRIPTION

UCD4002B NOR gate provides the system designer with direct implementation of the NOR function and supplements the existing family of CMOS gates. All inputs and outputs are buffered.

FEATURES

- * Propagation delay time=60ns at $C_L=50pF, V_{DD}=10V$
- * Buffered inputs and outputs
- * Maximum input current of $1\mu A$ at 18V
- * standardized symmetrical output characteristics
- * 100% tested for maximum quiescent current at 20V

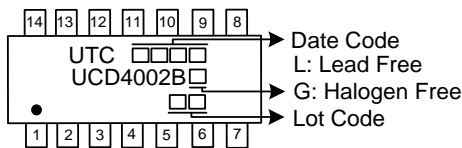


ORDERING INFORMATION

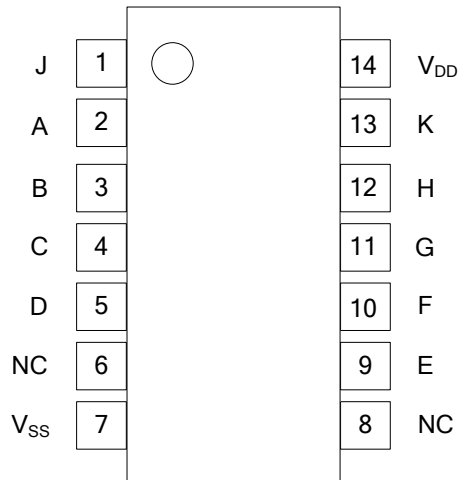
Ordering Number		Package	Packing
Lead Free	Halogen Free		
UCD4002BL-S14-R	UCD4002BG-S14-R	SOP-14	Tape Reel
UCD4002BL-P14-R	UCD4002BG-P14-R	TSSOP-14	Tape Reel

<p>UCD4002BG-S14-R</p> <ul style="list-style-type: none"> (1) Packing Type (2) Package Type (3) Green Package 	<ul style="list-style-type: none"> (1) R: Tape Reel (2) S14: SOP-14, P14: TSSOP-14 (3) G: Halogen Free and Lead Free, L: Lead Free
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MARKING



PIN CONFIGURATION

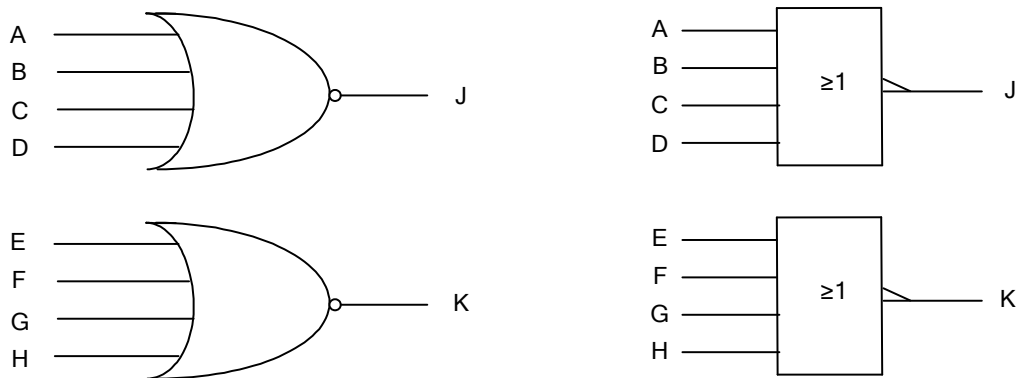


FUNCTION TABLE

INPUT	INPUT	INPUT	INPUT	INPUT	INPUT	INPUT	INPUT	OUTPUT	OUTPUT
A	B	C	D	E	F	G	H	K	J
L	L	L	L	L	L	L	L	H	H
H	X	X	X	H	X	X	X	L	L
X	H	X	X	X	H	X	X	L	L
X	X	H	X	X	X	H	X	L	L
X	X	X	H	X	X	X	H	L	L

NOTE: X = DON'T CARE CASE

LOGIC DIAGRAM



■ **ABSOLUTE MAXIMUM RATING** ($T_A = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	-0.5 ~ 20	V
Input Voltage	V_{IN}	-0.5 ~ $V_{CC}+0.5$	V
Output Voltage	V_{OUT}	-0.5 ~ $V_{CC}+0.5$	V
Power Dissipation($T_A = 55^\circ\text{C}$)	P_D	500	mW
Storage Temperature	T_{STG}	-65 ~ + 150	$^\circ\text{C}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.
Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ **RECOMMENDED OPERATING CONDITIONS**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{DD}		3		18	V
Operating Temperature	T_{OPR}		-40		+125	$^\circ\text{C}$

■ **ELECTRICAL CHARACTERISTICS** ($T_A = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Input Voltage	V_{IH}	$V_{DD} = 5\text{V}, V_O = 0.5\text{V}$	3.5			V
		$V_{DD} = 10\text{V}, V_O = 1.0\text{V}$	7.0			
		$V_{DD} = 15\text{V}, V_O = 1.5\text{V}$	11.0			
Low-Level Input Voltage	V_{IL}	$V_{DD} = 5\text{V}, V_O = 4.5\text{V}$			1.5	V
		$V_{DD} = 10\text{V}, V_O = 9.0\text{V}$			3.0	
		$V_{DD} = 15\text{V}, V_O = 13.5\text{V}$			4.0	
High-Level Output Voltage	V_{OH}	$V_{DD} = 5\text{V}, \text{No Load}$	4.95	5		V
		$V_{DD} = 10\text{V}, \text{No Load}$	9.95	10		
		$V_{DD} = 15\text{V}, \text{No Load}$	14.95	15		
Low-Level Output Voltage	V_{OL}	$V_{DD} = 5\text{V}, \text{No Load}$		0	0.05	V
		$V_{DD} = 10\text{V}, \text{No Load}$		0	0.05	
		$V_{DD} = 15\text{V}, \text{No Load}$		0	0.05	
High-Level Output Current (Note)	I_{OH}	$V_{DD} = 5\text{V}, V_O = 4.6\text{V}$	-0.51	-1.0		mA
		$V_{DD} = 5\text{V}, V_O = 2.5\text{V}$	-1.6	-3.2		
		$V_{DD} = 10\text{V}, V_O = 9.5\text{V}$	-1.3	-2.6		
		$V_{DD} = 15\text{V}, V_O = 13.5\text{V}$	-3.4	-6.8		
Low-Level Output Current (Note)	I_{OL}	$V_{DD} = 5\text{V}, V_O = 0.4\text{V}$	0.51	1		mA
		$V_{DD} = 10\text{V}, V_O = 0.5\text{V}$	1.3	2.6		
		$V_{DD} = 15\text{V}, V_O = 1.5\text{V}$	3.4	6.8		
Input Leakage Current	$I_{I(LEAK)}$	$V_{DD} = 15\text{V}, V_{IN} = V_{DD} \text{ or } \text{GND}$			± 0.1	μA
Quiescent Supply Current	I_{DD}	$V_{DD} = 5\text{V}, V_{IN} = V_{DD} \text{ or } V_{SS}, I_{OUT} = 0$		0.01	0.25	μA
		$V_{DD} = 10\text{V}, V_{IN} = V_{DD} \text{ or } V_{SS}, I_{OUT} = 0$		0.01	0.5	
		$V_{DD} = 15\text{V}, V_{IN} = V_{DD} \text{ or } V_{SS}, I_{OUT} = 0$		0.01	1.0	
		$V_{DD} = 20\text{V}, V_{IN} = V_{DD} \text{ or } V_{SS}, I_{OUT} = 0$		0.02	5.0	

Note: I_{OL} and I_{OH} are tested one output at a time.

■ SWITCHING CHARACTERISTICS

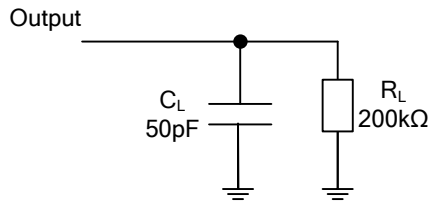
($T_A = 25^\circ\text{C}$, Input t_r , $t_f = 20\text{ns}$, $C_L = 50\text{pf}$, $R_L = 200\text{k}\Omega$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay from Input(A or B) to Output(Y)	t_{PLH}	$V_{DD}=5\text{V}$		125	250	ns
		$V_{DD}=10\text{V}$		60	120	
		$V_{DD}=15\text{V}$		45	90	
	t_{PHL}	$V_{DD}=5\text{V}$		125	250	
		$V_{DD}=10\text{V}$		60	120	
		$V_{DD}=15\text{V}$		45	90	
Transition Time	t_{TLH}/t_{THL}	$V_{DD}=5\text{V}$		100	200	ns
		$V_{DD}=10\text{V}$		50	100	
		$V_{DD}=15\text{V}$		40	80	

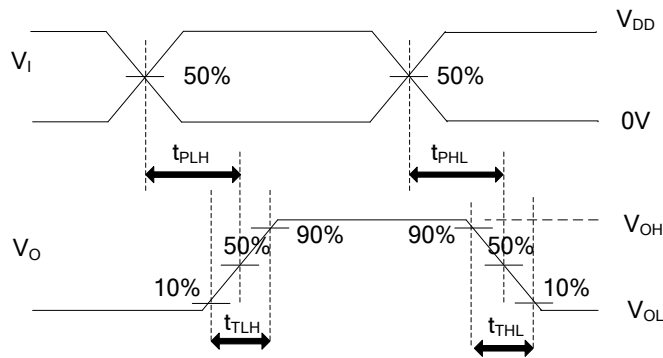
■ OPERATING CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Average Input Capacitance	C_{IN}	Any Input		5	7.5	pF

■ TEST CIRCUIT AND WAVEFORMS



Definitions for test circuit



Propagation Delay Times

Note: C_L includes probe and jig capacitance.

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