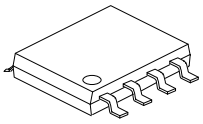
10A, 30V N-CHANNEL ENHANCEMENT MODE MOSFET



SOP-8

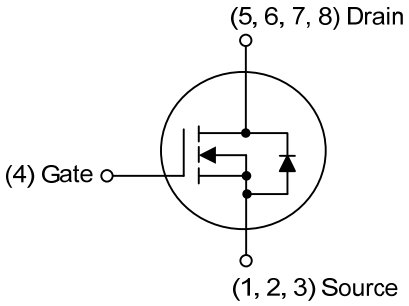
■ DESCRIPTION

The UTC **UT4466** is an N-channel Power FET, it uses UTC's advanced technology to provide customers a minimum on-state resistance, high switching speed and low gate charge.

■ FEATURES

* $R_{DS(ON)}$ < 15mΩ @ V_{GS}=10V, I_D=10A
* High switching speed
* Low gate charge (Typ.=10.5nC)

■ SYMBOL



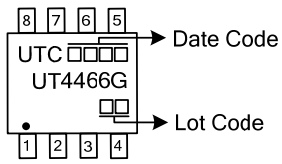
■ ORDERING INFORMATION

Ordering Number	Package	Pin Assignment								Packing
		1	2	3	4	5	6	7	8	
UT4466G-S08-R	SOP-8	S	S	S	G	D	D	D	D	Tape Reel

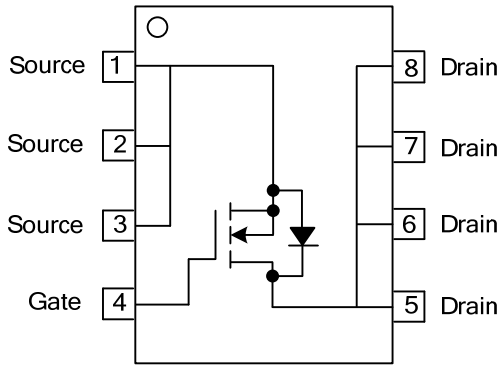
Note: Pin Assignment: G: Gate D: Drain S: Source

UT4466G-S08-R (1) Packing Type (2) Package Type (3) Green Package	(1) R: Tape Reel (2) S08: SOP-8 (3) G: Halogen Free and Lead Free

■ MARKING



■ PIN CONFIGURATION



■ ABSOLUTE MAXIMUM RATINGS (T_A=25°C, unless otherwise specified)

PARAMETER			SYMBOL	RATINGS	UNIT
Drain-Source Voltage			V_{DSS}	30	V
Gate-Source Voltage			V_{GSS}	±25	V
Drain Current	Continuous(Note 2)	T_A=25°C	I_D	10	A
		T_A=85°C		6	A
	Pulsed (Note 3)		I_{DM}	60	A
Avalanche Current (Note 3, 4)			I_{AR}	16	A
Repetitive Avalanche Energy (Note 3, 4)		L=0.1mH	E_{AR}	12.8	mJ
Power Dissipation (Note 2)			P_D	1.42	W
Junction Temperature			T_J	-55~+150	°C
Storage Temperature Range			T_{STG}	-55~+150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Device mounted on FR-4 substrate PC board with minimum recommended pad layout in a still air environment @ T_A=25°C. The value in any given application depends on the user's specific board design.
3. Repetitive rating, pulse width limited by junction temperature.
4. I_{AR} and E_{AR} rating are based on low frequency and duty cycles to keep T_J=25°C

■ THERMAL CHARACTERISTICS (T_A=25°C, unless otherwise specified)

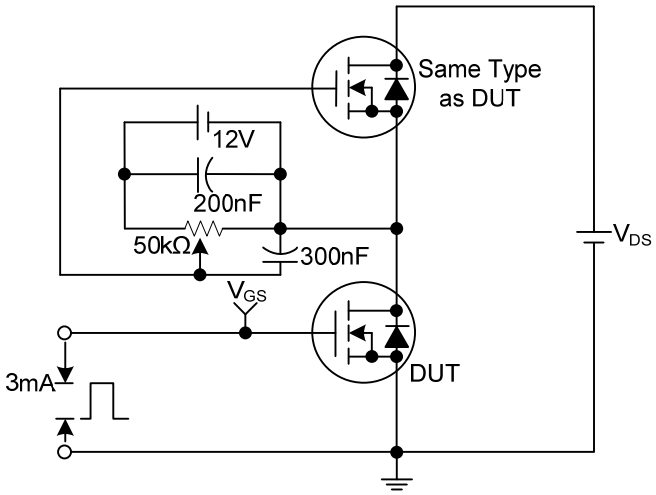
PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient (Note 1)	θ_{JA}	88.4	°C/W

■ ELECTRICAL CHARACTERISTICS (T_A=25°C, unless otherwise specified)

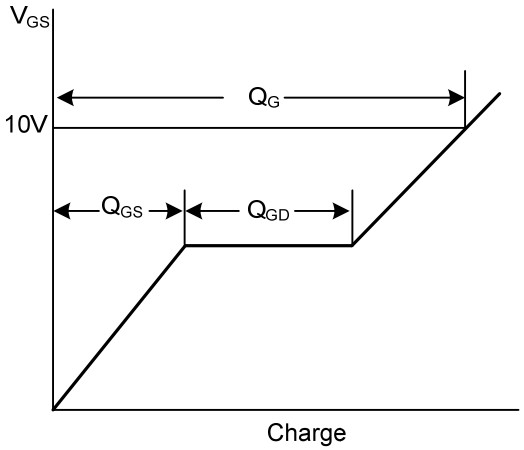
PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS (Note 1)							
Drain-Source Breakdown Voltage		BV_{DSS}	I_D=250μA, V_{GS}=0V	30			V
Drain-Source Leakage Current		I_{DSS}	V_{DS}=30V, V_{GS}=0V			1	μA
Gate-Source Leakage Current	Forward	I_{GSS}	V_{GS}=+25V, V_{DS}=0V			+100	nA
	Reverse		V_{GS}=-25V, V_{DS}=0V			-100	nA
ON CHARACTERISTICS (Note 1)							
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=250μA	1.0	1.45	2.4	V
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	V_{GS}=10V, I_D=10A		15	23	mΩ
			V_{GS}=4.5V, I_D=7.5A		25	33	mΩ
Forward Transfer Admittance		$\|Y_{FS}\|$	V_{DS}=5V, I_D=10A		2.5		S
DYNAMIC PARAMETERS (Note 2)							
Input Capacitance		C_{ISS}	V_{GS}=0V, V_{DS}=15V, f=1.0MHz		478.9		pF
Output Capacitance		C_{OSS}			96.7		pF
Reverse Transfer Capacitance		C_{RSS}			61.4		pF
SWITCHING PARAMETERS							
Gate Resistance		R_G	V_{DS}=0V, V_{GS}=0V, f=1MHz	0.4	1.1	1.6	Ω
Total Gate Charge		Q_G	V_{GS}=4.5V, V_{DS}=15V, I_D=10A		5.0	8	nC
Total Gate Charge		Q_G	V_{GS}=10V, V_{DS}=15V, I_D=10A		10.5	17	nC
Gate to Source Charge		Q_{GS}			1.8		nC
Gate to Drain Charge		Q_{GD}			1.6		nC
Turn-ON Delay Time		$t_{D(ON)}$	V_{DS}=15V, V_{GS}=10V, R_G=3Ω, R_L=1.5Ω		2.9		ns
Rise Time		t_R			7.9		ns
Turn-OFF Delay Time		$t_{D(OFF)}$			14.6		ns
Fall-Time		t_F			3.1		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Drain-Source Diode Forward Voltage		V_{SD}	I_S=1A, V_{GS}=0V		0.69	1	V

Notes: 1. Short duration pulse test used to minimize self-heating effect.
2. Guaranteed by design. Not subject to production testing.

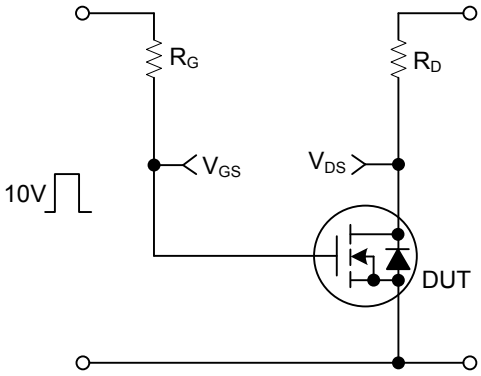
■ TEST CIRCUITS AND WAVEFORMS



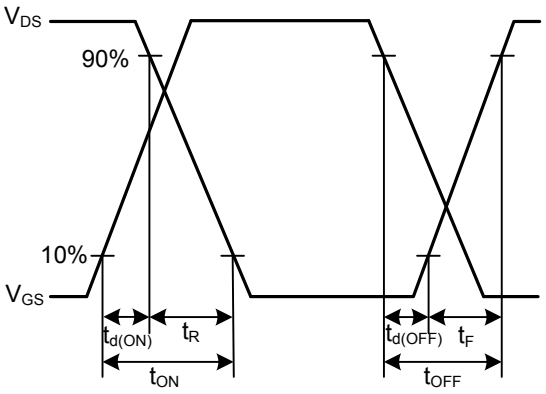
Gate Charge Test Circuit



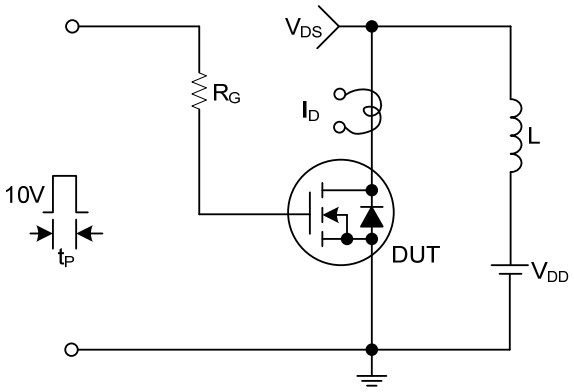
Gate Charge Waveforms



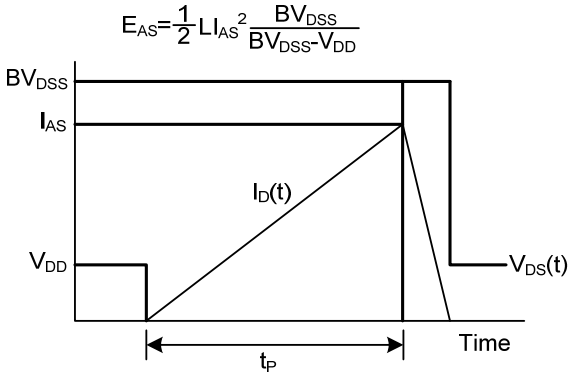
Resistive Switching Test Circuit



Resistive Switching Waveforms

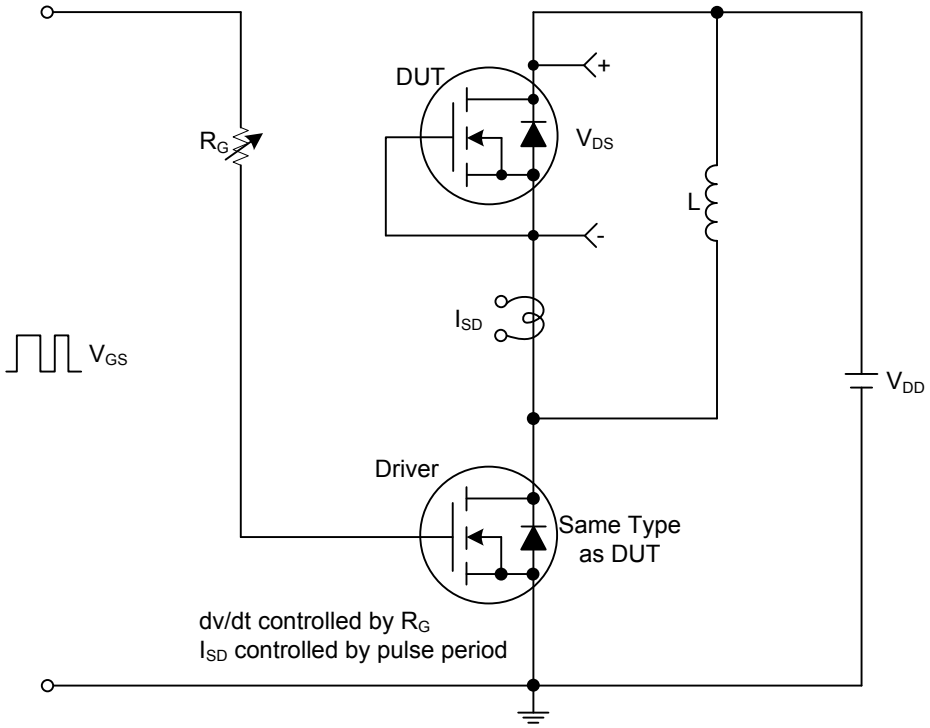


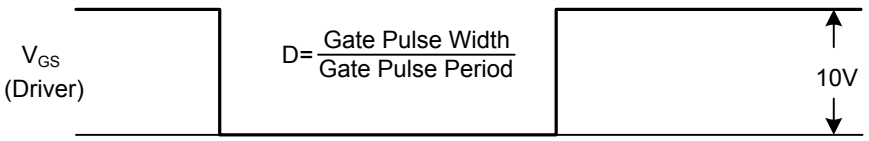
Unclamped Inductive Switching Test Circuit

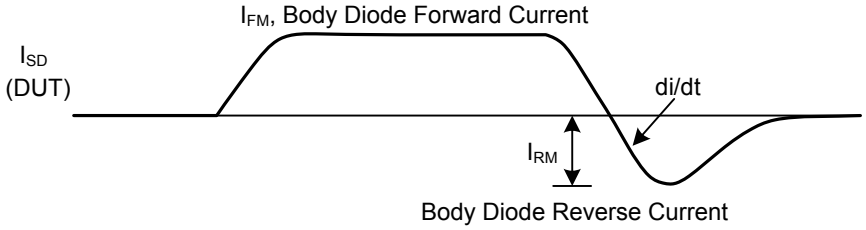


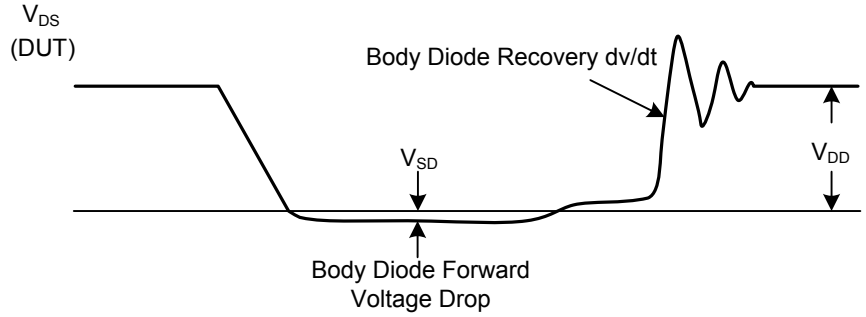
Unclamped Inductive Switching Waveforms

■ TEST CIRCUITS AND WAVEFORMS(Cont.)









Peak Diode Recovery dv/dt Test Circuit and Waveforms