

# U74HCT7046

**CMOS IC**

## PHASE LOCKED LOOP WITH VCO & LOCK DETECTOR

### ■ DESCRIPTION

The **U74HCT7046** is phase-locked-loop circuit that comprise a linear voltage-controlled oscillator (VCO), two-phase comparators (PC1, PC2), a lock detector, a common signal input amplifier and a common comparator input.

The lock detector capacitor should be connected between pin 15(CLD) and pin 8(GND).For a frequency range of 100kHz to 10MHz,the lock detector capacitor must be 1000pF to 10pF, respectively.

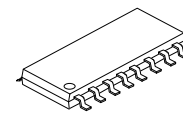
The signal can be directly coupled to large voltage signals, or with a series capacitor coupled to small signals. Small voltage signals can be kept within the linear region of the input amplifiers with a self-bias input circuit. The **U74HCT7046** and a passive low-pass filter form a second-order loop PLL. With a linear op-amp, the VCO achieves excellent linearity.

The VCO requires external capacitor and resistor. R1 (between R1 and GND) and capacitor C1 (between C1A and C1B) determine the frequency range of the VCO. R2 (between R2 and GND) enables the VCO to have a frequency offset if required.

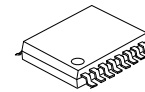
For the high input impedance of the VCO, the design of low-pass filters is simplified, and the designer has a wide choice of resistor/capacitor ranges. At pin 10 (DEM<sub>OUT</sub>), a demodulator output of the VCO input voltage is provided in order not to load the low-pass filter. In conventional techniques, the DEM<sub>OUT</sub> voltage is one threshold voltage lower than the VCO input voltage, but the DEM<sub>OUT</sub> voltage of U74HCT7046 equals the VCO input voltage. When DEM<sub>OUT</sub> is used, a load resistor (RS) should be connected from DEM<sub>OUT</sub> to GND; but if unused, DEM<sub>OUT</sub> should be left open. The VCO output (VCO<sub>OUT</sub>) can be connected directly or via a frequency-divider to the comparator input (COMP<sub>IN</sub>). If the VCO input is held at a constant DC level, the VCO output signal has a duty factor of 50% (maximum expected deviation 1%). A LOW level at the inhibit input (INH) enables the VCO and demodulator, while a HIGH level turns both off to minimize standby power consumption.

### ■ FEATURES

- \* Operating Power Supply Voltage Range: Digital Section 4.5 to 5.5 V  
VCO Section 4.5 to 5.5 V
- \* Up to 18 MHz (typ.) Centre Frequency at V<sub>CC</sub> = 5V
- \* Excellent V<sub>CO</sub> Frequency Linearity
- \* VCO-Inhibit Control For ON/OFF Keying and for Low Standby Power Consumption
- \* Minimal Frequency Drift
- \* Zero Voltage Offset due to OP-Amp Buffering



SOP-16



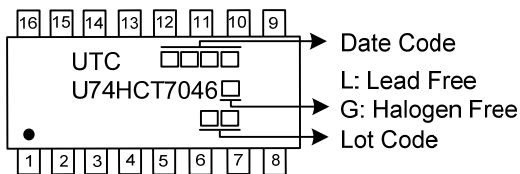
TSSOP-16

■ ORDERING INFORMATION

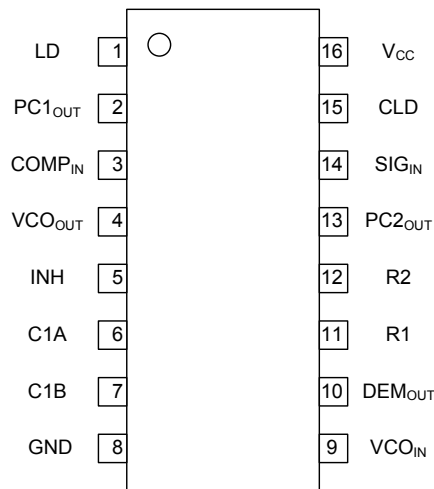
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74HCT7046L-S16-R	U74HCT7046G-S16-R	SOP-16	Tape Reel
U74HCT7046L-S16-T	U74HCT7046G-S16-T	SOP-16	Tube
U74HCT7046L-P16-R	U74HCT7046G-P16-R	TSSOP-16	Tape Reel
U74HCT7046L-P16-T	U74HCT7046G-P16-T	TSSOP-16	Tube

<p>U74HCT7046G-S16-R</p> <p>(1) Packing Type (2) Package Type (3) Green Package</p>	<p>(1) R: Tape Reel (2) S16: SOP-16, P16: TSSOP-16 (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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■ MARKING



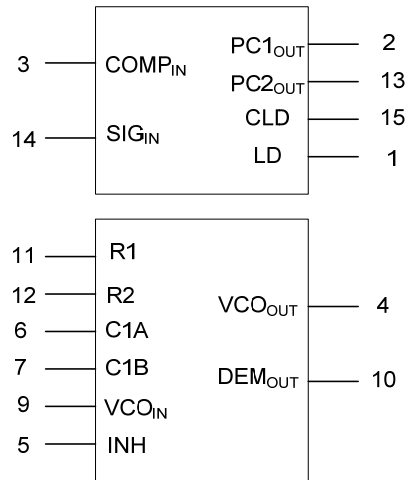
## PIN CONFIGURATION



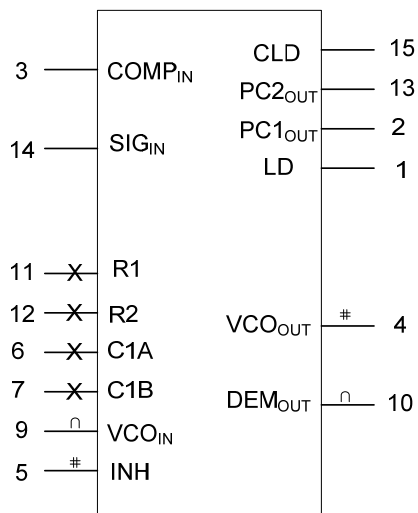
### ■ PIN DESCRIPTION

PIN NO	SYMBOL	FUNCTION
1	LD	Lock Detector Output(Active High)
2	PC1 <sub>OUT</sub>	Phase comparator 1output
3	COMP <sub>IN</sub>	Comparator input
4	VCO <sub>OUT</sub>	VCO output
5	INH	Inhibit input
6	C1 <sub>A</sub>	Capacitor C1 connection A
7	C1 <sub>B</sub>	Capacitor C1 connection B
8	GND	Ground(0V)
9	VCO <sub>IN</sub>	VCO input
10	DEM <sub>OUT</sub>	Demodulator output
11	R1	Resistor R1 connection
12	R2	Resistor R2 connection
13	PC2 <sub>OUT</sub>	Phase comparator 2 output
14	SIG <sub>IN</sub>	Signal input
15	CLD	Lock Detector Capacitor Input
16	V <sub>CC</sub>	Positive supply voltage

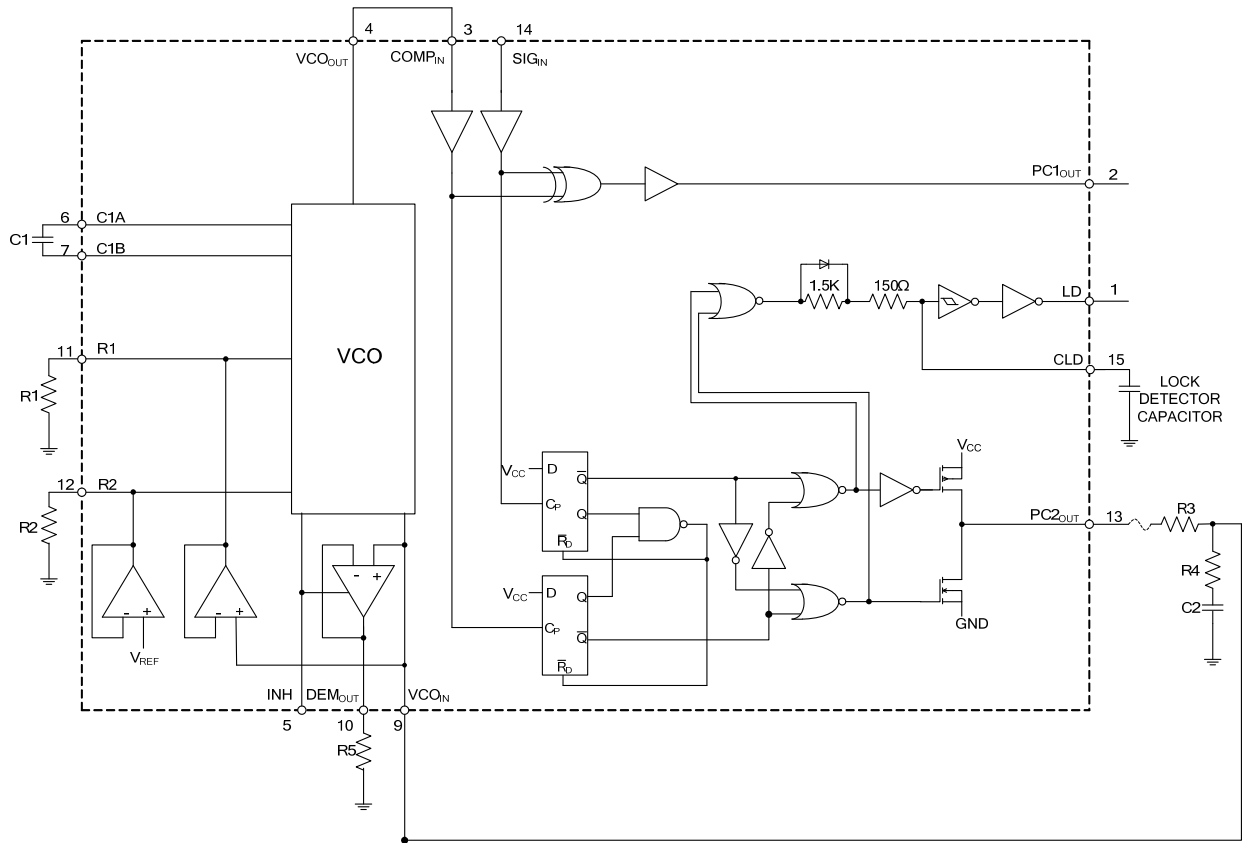
■ LOGIC SYMBOL



■ IEC SYMBOL



## LOGIC DIAGRAM



## ■ ABSOLUTE MAXIMUM RATING (Note 2)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNIT
Supply Voltage	$V_{CC}$		-0.5 ~ +7.0	V
Input Voltage	$V_{IN}$		-0.5 ~ $V_{CC}+0.5$	V
Output Voltage	$V_{OUT}$	Active Mode	-0.5 ~ $V_{CC}+0.5$	V
Continuous Output Current	$I_{OUT}$	$V_{OUT}=0V \sim V_{CC}$	±25	mA
Input Clamp Current	$I_{IK}$	$V_{IN}<0.5V$ or $V_{IN}>V_{CC}+0.5V$	±20	mA
Output Clamp Current	$I_{OK}$	$V_{OUT}\leq 0.5V$ or $V_{OUT}>V_{CC}+0.5V$	±20	mA
Continuous $V_{CC}$ or GND Current	$I_{CC}$		±50	mA
Storage Temperature Range	$T_{STG}$		-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.  
 2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## ■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Supply Voltage	$V_{CC}$		4.5	5.0	5.5	V
DC Supply Voltage if VCO Section is not used	$V_{CC}$		4.5	5.0	5.5	V
DC Input Voltage Range	$V_{IN}$		0		$V_{CC}$	V
DC Output Voltage Range	$V_{OUT}$		0		$V_{CC}$	V
Input Rise and Fall Times (Pin 5)	$t_R, t_F$	$V_{CC} = 4.5V$		6.0	500	ns
Ambient Operating Temperature	$T_{OPR}$	see DC and AC CHARACTERISTICS	-40		+85	°C
			-40		+125	°C

## ■ DC CHARACTERISTICS ( $T_A = 25^\circ C$ , unless otherwise specified)

**Quiescent Supply Current** (Voltages are referenced to GND, Ground = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Quiescent Supply Current	$I_{CC}$	$V_{CC}=5.5V, V_I = V_{CC}$ or GND			8.0	μA
Additional Quiescent Device Current Per Input Pin:1 Unit Load	$\Delta I_{CC}$	$V_{CC}=4.5V \sim 5.5V, V_I = V_{CC} - 2.1V$ (Pin 5 is excluded)		100	360	μA

## Phase Comparator Section

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Coupled (HIGH Level Input Voltage $SIG_{IN}, COMP_{IN}$ )	$V_{IH}$	$V_{CC}=4.5V$	3.15	2.4		V
DC Coupled (LOW Level Input Voltage $SIG_{IN}, COMP_{IN}$ )	$V_{IL}$	$V_{CC}=4.5V$		2.1	1.35	V
HIGH Level Output Voltage (LD, $PC_{NOUT}$ ) CMOS Loads	$V_{OH}$	$V_I = V_{IH}$ or $V_{IL}, V_{CC}=4.5V, -I_{OUT} = 20\mu A$	4.4	4.5		V
HIGH Level Output Voltage (LD, $PC_{NOUT}$ ) CMOS Loads	$V_{OH}$	$V_I = V_{IH}$ or $V_{IL}, V_{CC}=4.5V, -I_{OUT} = 4.0 mA$	3.98	4.32		V
LOW Level Output Voltage (LD, $PC_{NOUT}$ ) TTL Loads	$V_{OL}$	$V_I = V_{IH}$ or $V_{IL}, V_{CC}=4.5V, -I_{OUT} = 20\mu A$		0	0.1	V
LOW Level Output Voltage (LD, $PC_{NOUT}$ ) TTL Loads	$V_{OL}$	$V_I = V_{IH}$ or $V_{IL}, V_{CC}=4.5V, -I_{OUT} = 4.0 mA$		0.15	0.26	V
Input Leakage Current ( $SIG_{IN}, COMP_{IN}$ )	$\pm I_{IN}$	$V_I = GND$ to $V_{CC}, V_{CC}=5.5V$			±30	μA
3-State (OFF-state current $PC2_{OUT}$ )	$\pm I_{OZ}$	$V_{OUT} = V_{CC}$ or GND, $V_I = V_{IH}$ or $V_{IL}, V_{CC}=5.5V$			±0.5	μA
Input Resistance ( $SIG_{IN}, COMP_{IN}$ )	$R_{IN}$	$V_{CC}=4.5V, V_{IN}$ at self-bias operating point, $\Delta V_I = 0.5V$ (Fig. 7)		250		kΩ

## ■ DC CHARACTERISTICS (Cont.)

### VCO Section (Voltages are Referenced to GND, Ground=0V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
HIGH Level Input Voltage INH	$V_{IH}$	$V_{CC}=4.5V\sim 5.5V$	2	1.6		V
LOW Level Input Voltage INH	$V_{IL}$	$V_{CC}=4.5V\sim 5.5V$		1.2	0.8	V
HIGH Level Output Voltage VCO <sub>OUT</sub>	$V_{OH}$	$V_I=V_{IH}$ or $V_{IL}$ $V_{CC}=4.5V, -I_{OUT} = 20\mu A$	4.4	4.5		V
HIGH Level Output Voltage VCO <sub>OUT</sub>	$V_{OH}$	$V_{CC}=4.5V, -I_{OUT} = 4.0 Ma$ $V_I=V_{IH}$ or $V_{IL}$	3.9	4.3		V
LOW Level Output Voltage VCO <sub>OUT</sub>	$V_{OL}$	$V_I=V_{IH}$ or $V_{IL}$ $V_{CC}=4.5V, I_{OUT} = 20\mu A$		0	0.1	V
LOW Level Output Voltage VCO <sub>OUT</sub>	$V_{OL}$	$V_I=V_{IH}$ or $V_{IL}$ $V_{CC}=4.5V, I_{OUT} = 4.0 mA$		0.1 5	0.26	V
LOW Level Output Voltage C1 <sub>A</sub> , C1 <sub>B</sub>	$V_{OL}$	$V_I=V_{IH}$ or $V_{IL}$ $V_{CC}=4.5V, I_{OUT} = 4.0 mA$			0.4	V
Input Leakage Current(INH, VCO <sub>IN</sub> )	$\pm I_{IN}$	$V_{CC}=5.5V, V_I=GND$ to $V_{CC}$			$\pm 0.1$	$\mu A$
Resistance Range	R1 / R2	$V_{CC}=4.5V$ (Note1)	3.0		300	k $\Omega$
Capacitor Range	C1	$V_{CC}=4.5V$ (no limit Max.)	40			pF
Operating Voltage Range at VCO <sub>IN</sub>	$V_{VCOIN}$	$V_{CC}=4.5V$ , Over the range specified for R1; for linearity (Fig10)	1.1		3.4	V

Note: 1. The parallel value of R1 and R2 should be more than 2.7 k $\Omega$ . Optimum performance is achieved when R1 and/ or R2 are/is>10 k $\Omega$ .

### Demodulator Section (Voltages are Referenced to GND (Ground=0V))

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resistor Range	$R_S$	$V_{CC}=4.5V$ , At $R_S>300k\Omega$ the leakage current can influence $V_{DEMOUT}$	50		300	k $\Omega$
Offset Voltage VCO <sub>IN</sub> to V <sub>DEMOUT</sub>	$V_{OFF}$	$V_{CC}=4.5V, V_I = V_{VCOIN} = 1/2 V_{CC}$ , values taken over $R_S$ range		$\pm 20$		mV
Dynamic Output Resistance at DEM <sub>OUT</sub>	$R_D$	$V_{CC}=4.5V, V_{DEMOUT} = 1/2 V_{CC}$		25		$\Omega$

## ■ AC CHARACTERISTICS ( $T_A = 25^\circ C$ , unless otherwise specified)

### Phase Comparator Section (GND=0V, $t_R=t_F=6ns, C_L=50pF$ )

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay SIG <sub>IN</sub> , COMP <sub>IN</sub> to PC1 <sub>OUT</sub>	$t_{PHL} / t_{PLH}$	$V_{CC}=4.5V$ (Fig.8)		21	40	ns
Output Transition time	$t_{THL} / t_{TLH}$	$V_{CC}=4.5V$ (Fig.8)		7	15	ns
3-State Output Enable Time SIG <sub>IN</sub> , COMP <sub>IN</sub> to PC2 <sub>OUT</sub>	$t_{PZH} / t_{PZL}$	$V_{CC}=4.5V$ (Fig.9)		27	56	ns
3-State Output Disable Time SIG <sub>IN</sub> , COMP <sub>IN</sub> to PC2 <sub>OUT</sub>	$t_{PHZ} / t_{PLZ}$	$V_{CC}=4.5V$ (Fig.9)		35	65	ns
AC Coupled Input Sensitivity (Peak-To-Peak Value) at SIG <sub>IN</sub> or COMP <sub>IN</sub>	$V_{IN(P-P)}$	$V_{CC}=4.5V (f_i = 1MHz)$		15		mV

### VCO Section (GND=0V, $t_R=t_F=6ns, C_L=50pF$ )

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency Stability with Temperature Change	$\Delta f/T$	$V_{CC}=4.5V, V_{IN}=V_{VCOIN}=1/2 V_{CC}$ , $R1=100k\Omega, R2=\infty, C1=100pF$		0.15		%/K
VCO Centre Frequency (duty Factor = 50%)	$f_o$	$V_{CC}=4.5V, V_{VCOIN} = 1/2 V_{CC}$ , $R1=3k\Omega, R2 = \infty, C1=40pF$	11	17		MHz
VCO Frequency Linearity	$\Delta f_{VCO}$	$V_{CC}=4.5V, R1=100k\Omega$ , $R2=\infty, C1=100pF$ (Fig.10)		0.4		%
Duty factor at VCO <sub>OUT</sub>	$\delta_{VCO}$	$V_{CC}=4.5V$		50		%

■ PHASE COMPARATORS.

If the signal swing is between the standard HC family input logic levels, the signal input (SIG<sub>IN</sub>) can be directly coupled to the self-biasing amplifier at pin 14. Capacitive coupling is required for signals with smaller swings.

**Phase comparator 1 (PC1)**

This is an EXCLUSIVE-OR network. To obtain the maximum locking range, the signal and comparator input frequencies (f<sub>i</sub>) must have a 50% duty factor.

The transfer characteristic of PC1, assuming ripple (f<sub>r</sub> = 2f<sub>i</sub>) is suppressed, is:

$$V_{\text{DEMOUT}} = \frac{V_{\text{CC}}}{\pi} (\phi_{\text{SIGIN}} - \phi_{\text{COMPIN}})$$

Where V<sub>DEMOUT</sub> is the demodulator output at pin 10; V<sub>DEMOUT</sub> = V<sub>PC1OUT</sub> (via low-pass filter).

The phase comparator gain is:  $K_P = \frac{V_{\text{CC}}}{\pi} (V/r)$

As shown in Fig.1, the average output voltage from PC1, fed to the VCO input via the low-pass filter and seen at the demodulator output at pin 10 (V<sub>DEMOUT</sub>) is the resultant of the phase differences of signals (SIG<sub>IN</sub>) and the comparator input (COMP<sub>IN</sub>). The average of V<sub>DEMOUT</sub> is equal to V<sub>CC</sub>/2 when there is no signal or noise at SIG<sub>IN</sub> and with this input the VCO oscillates at the centre frequency (f<sub>0</sub>). As shown in Fig.2 it is the typical waveforms for the PC1 loop locked at f<sub>0</sub>.

$$V_{\text{DEMOUT}} = V_{\text{PC1OUT}} = \frac{V_{\text{CC}}}{\pi} (\phi_{\text{SIGIN}} - \phi_{\text{COMPIN}})$$

$$\phi_{\text{DEMOUT}} = (\phi_{\text{SIGIN}} - \phi_{\text{COMPIN}})$$

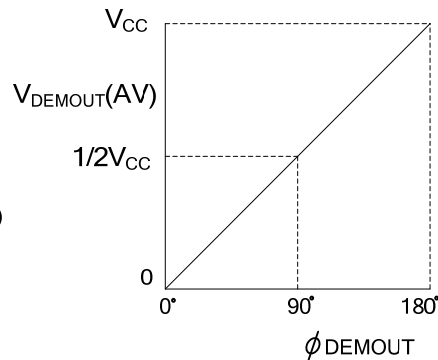


Fig.1 Phase comparator 1: average output voltage versus input phase difference.

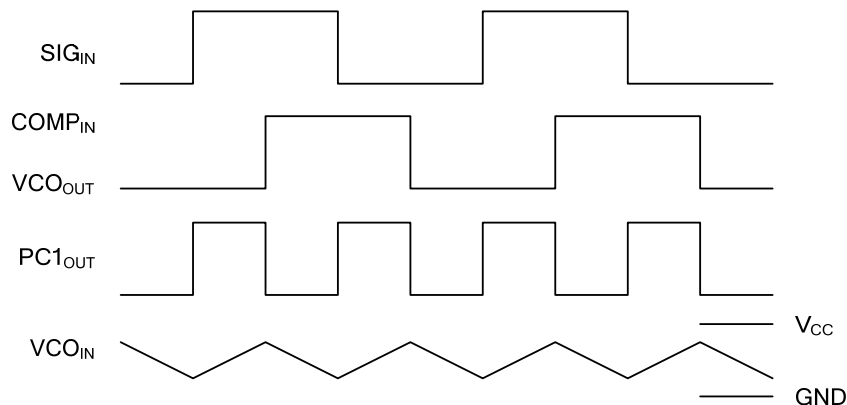


Fig.2 Typical waveforms for PLL using phase comparator 1, loop locked at f<sub>0</sub>.

The frequency capture range (2f<sub>c</sub>) is the frequency range of input signals on which the PLL will lock if it was initially out-of-lock. The frequency lock range (2f<sub>L</sub>) is the frequency range of input signals on which the loop will stay locked if it was initially in lock. The capture range is smaller or equal to the lock range.

With PC1, the low-pass filter characteristics determine the capture range which can be made as large as the lock range.

This configuration retains lock even with very noisy input signals. Typical behavior of this type of phase comparator is that it can lock to input frequencies close to the harmonics of the VCO centre frequency.



■ PHASE COMPARATORS (Cont.)

**Phase comparator 2 (PC2)**

This is a positive edge-triggered phase and frequency detector. If the PLL is using the comparator, the loop is controlled by positive signal transitions and the duty factors of SIG<sub>IN</sub> and COMP<sub>IN</sub> are not important. PC2 is comprised of two D-type flip-flops, control-gating and a 3-state output stage. The circuit function is as an up-down counter (Logic Diagram) for SIG<sub>IN</sub> causes an up-count and COMP<sub>IN</sub> causes a down-count.

The transfer function of PC2, assuming ripple (f<sub>r</sub> = f<sub>i</sub>) is suppressed, is

$$V_{\text{DEMOUT}} = \frac{V_{\text{CC}}}{4\pi} (\phi_{\text{SIGIN}} - \phi_{\text{COMPIN}})$$

where V<sub>DEMOUT</sub> is the demodulator output at pin 10; V<sub>DEMOUT</sub> = V<sub>PC2OUT</sub> (via low-pass filter).

The phase comparator gain is:  $K_P = \frac{V_{\text{CC}}}{4\pi} (V / r)$

As shown in Fig.3, V<sub>DEMOUT</sub> is the resultant of the initial phase differences of SIG<sub>IN</sub> and COMP<sub>IN</sub>. Typical waveforms for the PC2 loop locked at f<sub>0</sub> are shown in Fig.4.

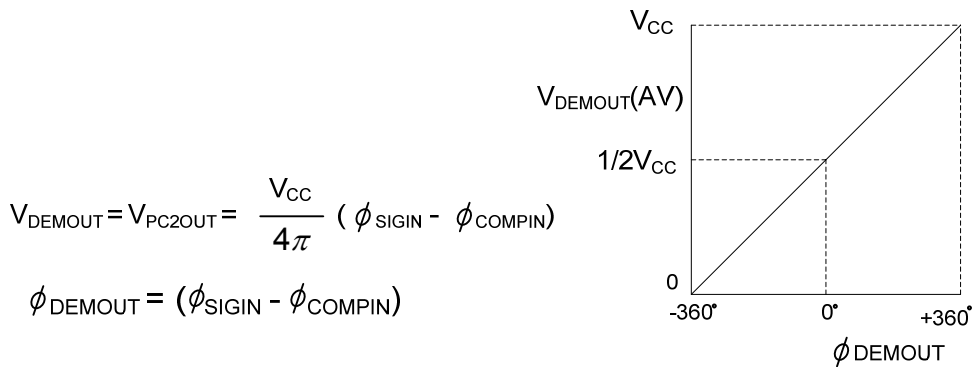


Fig.3 Phase comparator 2: average output voltage versus input phase difference.

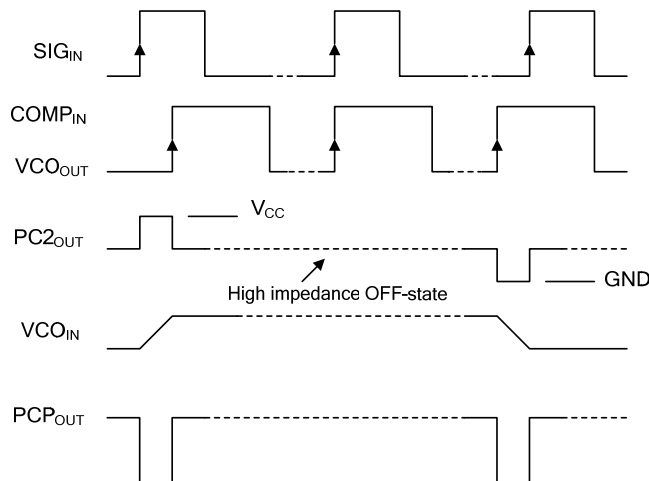


Fig.4 Typical waveforms for PLL using phase comparator 2, loop locked at f<sub>0</sub>.

## ■ PHASE COMPARATORS (Cont.)

If the frequencies of SIG<sub>IN</sub> and COMP<sub>IN</sub> are equal but the phase of SIG<sub>IN</sub> leads that of COMP<sub>IN</sub>, the p-type output driver at PC2<sub>OUT</sub> is held “ON” for a time corresponding to the phase difference ( $\phi_{\text{DEMOUT}}$ ). If the phase of SIG<sub>IN</sub> lags that of COMP<sub>IN</sub>, the n-type driver is held “ON”.

If the frequency of SIG<sub>IN</sub> is higher than that of COMP<sub>IN</sub>, the p-type output driver is held “ON” for most of the input signal cycle time, and for the remainder of the cycle both n and p-type drivers are “OFF” (3-state). If the frequency of SIG<sub>IN</sub> is lower than that of COMP<sub>IN</sub>, the n-type driver is held “ON” for most of the cycle. Then the voltage at the capacitor (C2) of the low-pass filter connected to PC2<sub>OUT</sub> varies until the signal and comparator inputs are equal in both phase and frequency. At this stable state the voltage on C2 remains constant as the PC2 output is in 3-state and the VCO input at pin 9 is a high impedance. Also in the condition, the signal at the phase comparator pulse output (PCP<sub>OUT</sub>) is a HIGH level, and it indicates a locked condition.

For PC2, there is no phase difference between SIG<sub>IN</sub> and COMP<sub>IN</sub> over the full frequency range of the VCO. And as the low-pass filter, the power dissipation is reduced because both p and n-type drivers are “OFF” for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range and this is independent of the low-pass filter. The VCO adjusts to its lowest frequency via PC2 when no signal present at SIG<sub>IN</sub>.

## ■ LOCK DETECTOR THEORY OF OPERATION

Detection of a locked condition is accomplished by a NOR gate and an envelope detector. When the PLL is in Lock, the output of the NOR gate is High and the lock detector output (Pin 1) is at a constant high level. As the loop tracks the signal on Pin 14 (signal in), the NOR gate outputs pulses whose widths represent the phase differences between the VCO and the input signal. The time between pulses will be approximately equal to the time constant of the VCO center frequency. During the rise time of the pulse, the diode across the 1.5k $\Omega$  resistor is forward biased and the time constant in the path that charges the lock detector capacitor is  $T = (150\Omega \times \text{CLD})$ .

During the fall time of the pulse the capacitor discharges through the 1.5k $\Omega$  and the 150 $\Omega$  resistors and the channel resistance of the n-device of the NOR gate to ground ( $T = (1.5\text{k}\Omega + 150\Omega + R_{\text{n-channel}}) \times \text{CLD}$ ).

The waveform present at the capacitor resembles a sawtooth. The lock detector capacitor value is determined by the VCO center frequency. The typical range of capacitor for a frequency of 10MHz is about 10pF and for a frequency of 100kHz is about 1000pF. As long as the loop remains locked and tracking, the level of the sawtooth will not go below the switching threshold of the Schmitt-trigger inverter. If the loop breaks lock, the width of the error pulse will be wide enough to allow the sawtooth waveform to go below threshold and a level change at the output of the Schmitt trigger will indicate a loss of lock. The lock detector capacitor also acts to filter out small glitches that can occur when the loop is either seeking or losing lock.

## ■ FIGURE REFERENCES FOR DC CHARACTERISTICS

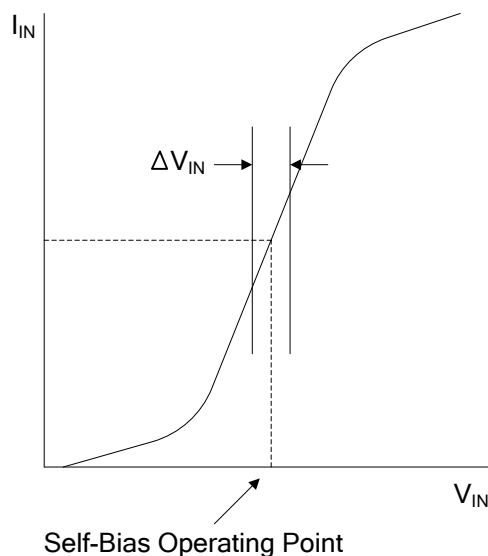


Fig.7 Typical input resistance curve at SIG<sub>IN</sub>, COMP<sub>IN</sub>.

■ AC WAVEFORMS

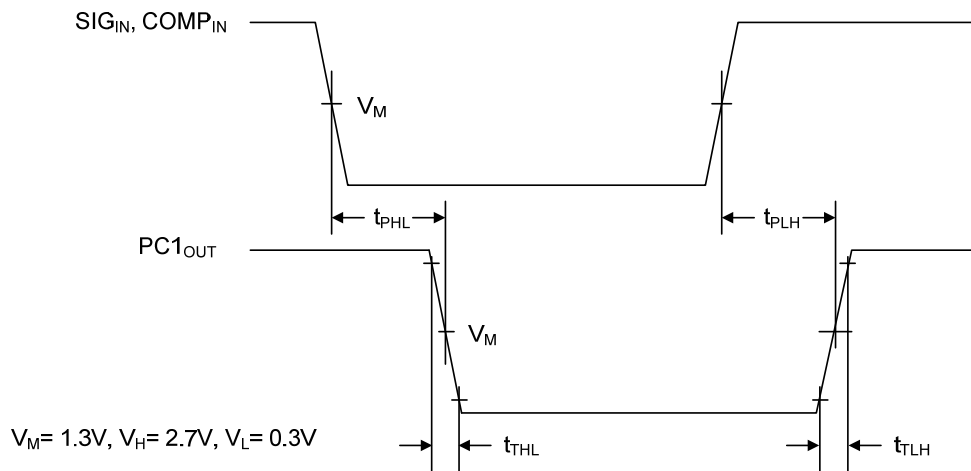


Fig.8 Waveforms showing input (SIG<sub>IN</sub>, COMP<sub>IN</sub>) to output (PC1<sub>OUT</sub>) propagation delays and the output transition times.

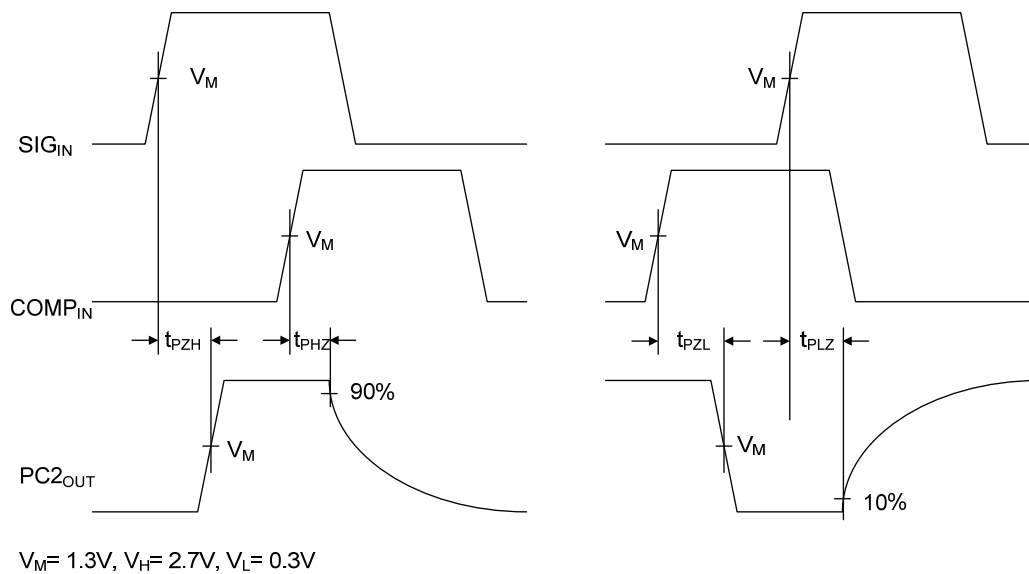


Fig.9 Waveforms showing the 3-state enable and disable times for PC2<sub>OUT</sub>.

■ AC WAVEFORMS (Cont.)

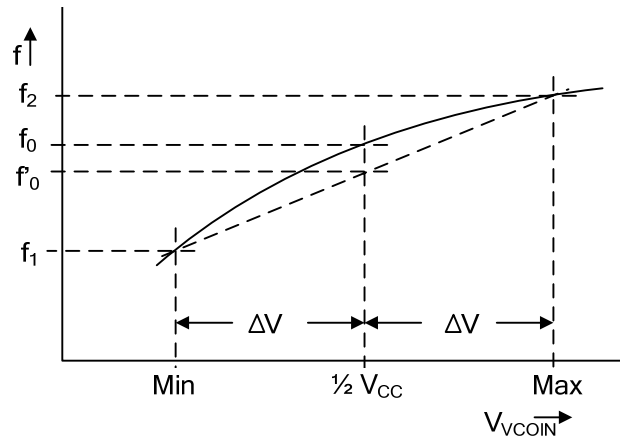


Fig.10 Definition of VCO frequency linearity:  $\Delta V = 0.5 \text{ V}$  over the VCC range:  
 for VCO linearity  $f'_0 = (f_1+f_2)/2$ , linearity  $(f'_0+f_0)/f_0 \times 100\%$

## ■ APPLICATION INFORMATION

This is a reference for the values of external components to be used with the **U74HCT7046** in a PLL system. The ranges of the values of the components:

Component	Value
R1	3 kΩ ~ 300 kΩ
R2	3 kΩ ~ 300 kΩ
R1+R2	Parallel value > 2.7 kΩ
C1	Greater than 40 pF

### VCO Frequency Without Extra Offset (Phase comparator: PC1, PC2)

Frequency Characteristic:

With  $R2 = \infty$  and  $R1$  between 3 kΩ and 300 kΩ, the characteristics of the VCO operation will be as shown in Fig.11 (Due to  $R1$ ,  $C1$  time constant a small offset remains when  $R2 = \infty$ ).

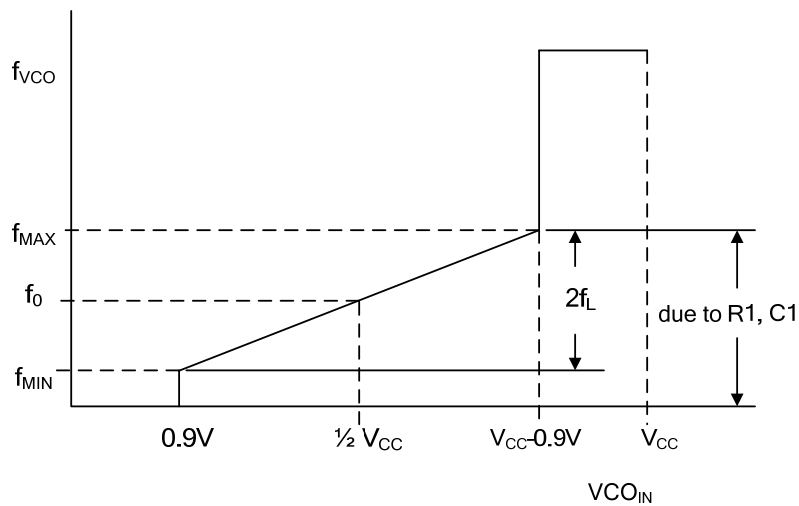


Fig.11 Frequency characteristic of VCO operating without offset:  
 $f_0$  = centre frequency;  $2f_L$  = frequency lock range.

■ APPLICATION INFORMATION(Cont.)

**VCO Frequency with Extra Offset** (Phase Comparator: PC1, PC2)

Frequency characteristic:

With R1 and R2 between 3 kΩ and 300 kΩ, the characteristics of the VCO operation will be as shown in Fig.12.

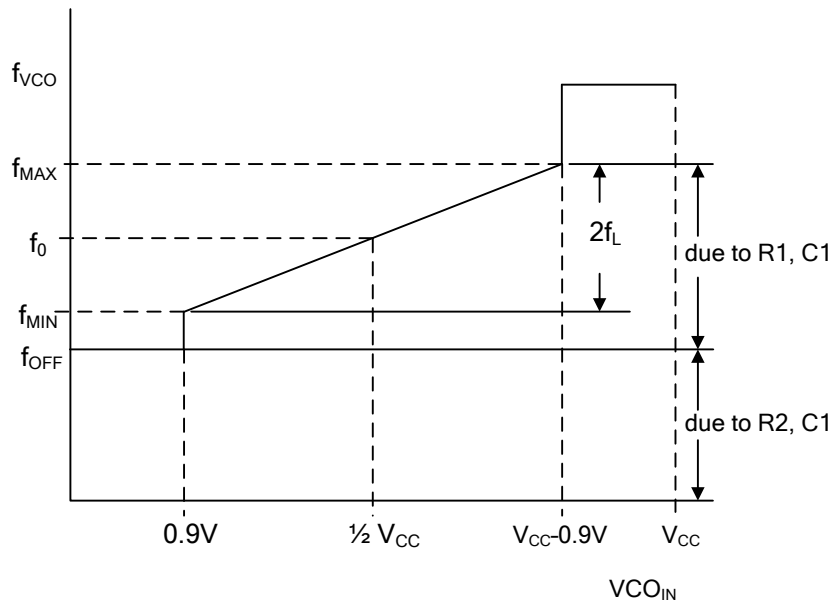


Fig.12 Frequency characteristic of VCO operating with offset:

$f_0$  = centre frequency;  $2f_L$  = frequency lock range.

PC1, PC2

Selection of R1, R2 and C1

Given  $f_0$  and  $f_L$ , determine the value of  $R1 \times C1$

Calculate  $f_{OFF}$  from the equation  $f_{OFF} = f_0 - 1.6f_L$

Obtain the values of C1 and R2

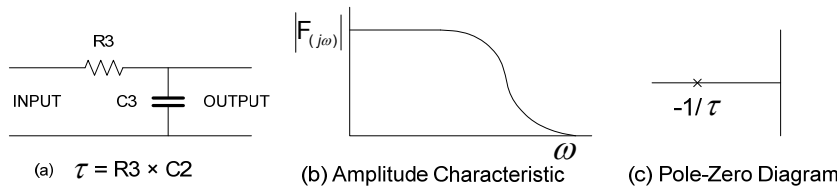
Calculate the value of R1 from the value of C1 and  $R1 \times C1$ .

Subject	Phase comparator	Design considerations
PLL Conditions with no Signal at the SIG <sub>IN</sub> Input	PC1	VCO adjusts to $f_0$ with $\phi_{DEMOUT} = 90^\circ$ and $V_{VCONIN} = 1/2 V_{CD}$ (Fig.1).
	PC2	VCO adjusts to $f_0$ with $\phi_{DEMOUT} = -360^\circ$ and $V_{VCONIN} = \text{min.}$ (Fig.3).

■ APPLICATION INFORMATION (Cont.)

**PLL Frequency Capture Range** (Phase comparator: PC1, PC2)

Loop filter component selection



A small capture range ( $2f_c$ ) is obtained if  $2f_c \approx \frac{1}{\pi} \sqrt{2\pi f_L / \tau}$

Fig. 13 Simple loop filter for PLL without offset;  $R3 \geq 500 \Omega$ .

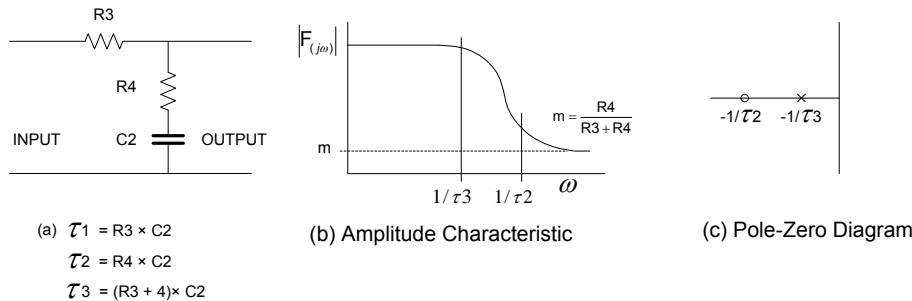


Fig. 14 Simple loop filter for PLL with offset;  $R3 + R4 \geq 500 \Omega$ .

Subject	Phase comparator	Design considerations
PLL Locks on Harmonics at Centre Frequency	PC1	Yes
	PC2	No
Noise Rejection at Signal Input	PC1	High
	PC2	Low
AC Ripple Content when PLL is Locked	PC1	$f_r = 2f_i$ , large ripple content at $\phi_{\text{DEMOUT}} = 90^\circ$
	PC2	$f_r = f_i$ , small ripple content at $\phi_{\text{DEMOUT}} = 0^\circ$

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