

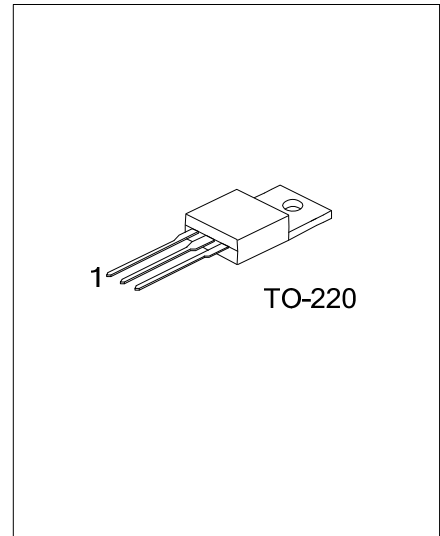


200 A, 20 V N-CHANNEL POWER MOSFET

DESCRIPTION

The UTC **UTT200N02** is an N-channel power MOSFET using UTC's advanced technology to provide customers with a minimum on-state resistance and superior switching performance.

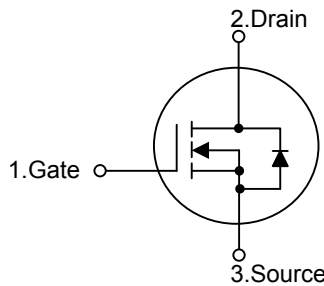
The UTC **UTT200N02** is generally applied in synchronous Rectification or DC to DC convertor.



FEATURES

- * $V_{DS} = 20V$
- * $I_D = 200A$
- * $R_{DS(ON)} = 2.0m\Omega(Typ.) @ V_{GS} = 10V$
- * Low Gate Charge (Typical 84nC)
- * High Switching Speed
- * High Power and Current Handling Capability
- * RoHS Compliant

SYMBOL



ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UTT200N02L-TA3-T	UTT200N02G-TA3-T	TO-220	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

UTT200N02L-TA3-T (1) Packing Type (2) Package Type (3) Lead Free	(1) T: Tube (2) TA3: TO-220 (3) G: Halogen Free, L: Lead Free
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■ ABSOLUTE MAXIMUM RATINGS ($T_c=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	20	V
Gate-Source Voltage		V_{GSS}	± 20	V
Drain Current	Continuous (Silicon Limited)	I_D	200 (Note 2)	A
	Pulsed (Note 3)	I_{DM}	800	A
Single Pulsed Avalanche Energy (Note 4)		E_{AS}	864	mJ
Peak Diode Recovery dv/dt (Note 5)		dv/dt	6.0	V/ns
Power Dissipation		P_D	214	W
Derate above 25°C			1.43	W/ $^\circ\text{C}$
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature Range		T_{STG}	-55~+175	$^\circ\text{C}$

Note: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 100A.

3. Repetitive Rating: Pulse width limited by maximum junction temperature

4. $L = 3\text{mH}$, $I_{AS} = 24\text{A}$, $V_{DD} = 20\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$

5. $I_{SD} \leq 200\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	62.5	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	0.7	$^\circ\text{C}/\text{W}$

■ ELECTRICAL CHARACTERISTICS (T_c=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	I _D =250μA, V _{GS} =0V	20			V
Breakdown Voltage Temperature Coefficient	ΔBV _{DSS} /ΔT _J	Reference to 25°C, I _D =250μA		30		mV/°C
Drain-Source Leakage Current	I _{DSS}	V _{DS} =20V, V _{GS} =0V			10	μA
Gate- Source Leakage Current	Forward	V _{GS} =+20V, V _{DS} =0V			+100	nA
	Reverse	V _{GS} =-20V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	1.0		3.0	V
Static Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =80A		2.0	2.4	mΩ
DYNAMIC PARAMETERS						
Input Capacitance	C _{ISS}	V _{GS} =0V, V _{DS} =25V, f=1.0MHz		5490	7300	pF
Output Capacitance	C _{OSS}			1220	1620	pF
Reverse Transfer Capacitance	C _{RSS}			155	233	pF
SWITCHING PARAMETERS						
Total Gate Charge at 10V	Q _{G(tot)}	V _{GS} =10V, V _{DS} =16V, I _D =80A (Note 1, 2)		84	109	nC
Gate to Source Charge	Q _{GS}			19		nC
Gate Charge Threshold to Plateau	Q _{GS2}			9.5		nC
Gate to Drain Charge	Q _{GD}			12		nC
Turn-ON Delay Time	t _{D(ON)}	V _{DD} =10V, I _D =80A, R _{GEN} =4.7Ω, V _{GS} =10V (Note 1, 2)		17	44	ns
Rise Time	t _R			8	26	ns
Turn-OFF Delay Time	t _{D(OFF)}			71	152	ns
Fall-Time	t _F			17	44	ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I _S				200	A
Maximum Body-Diode Pulsed Current	I _{SM}				800	A
Drain-Source Diode Forward Voltage	V _{SD}	I _{SD} =200A, V _{GS} =0V			1.3	V

Notes: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%

2. Essentially independent of operating temperature Typical Characteristics

■ TEST CIRCUITS AND WAVEFORMS

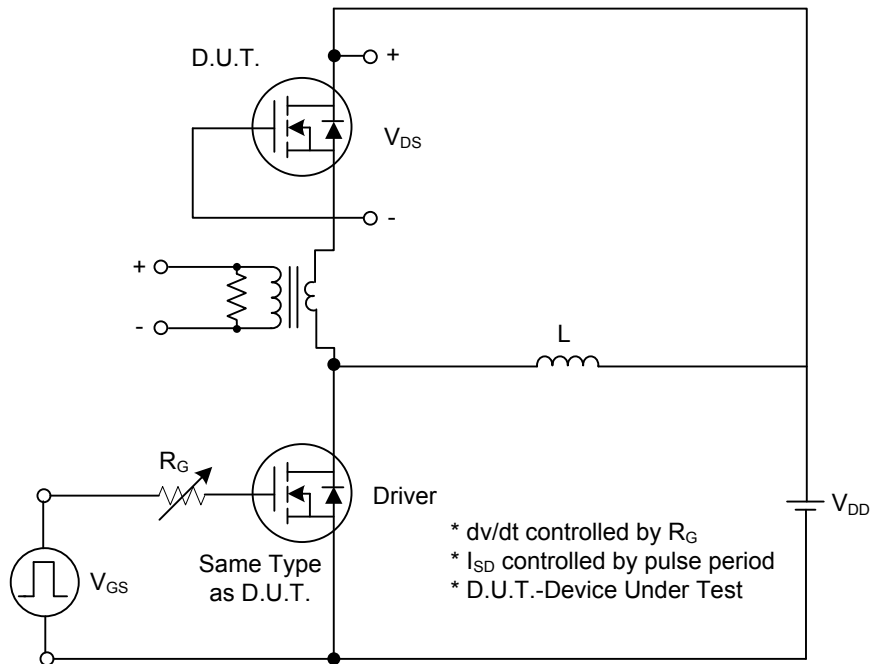


Fig. 1A Peak Diode Recovery dv/dt Test Circuit

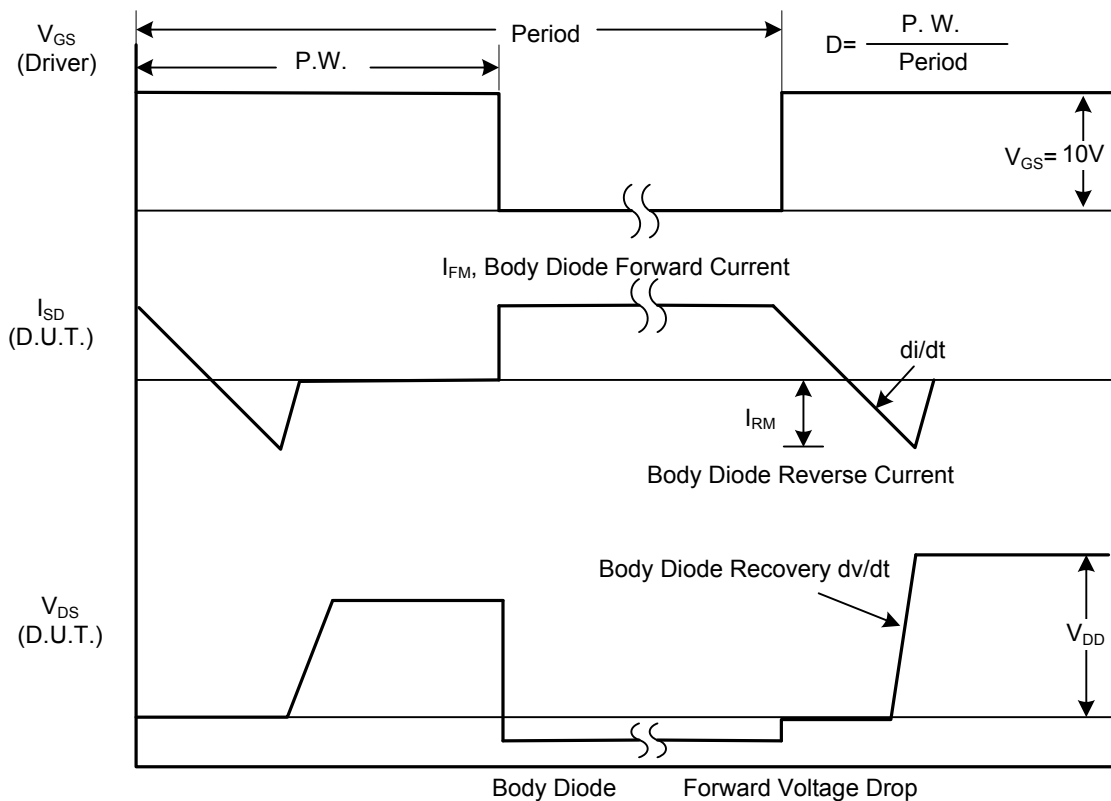


Fig. 1B Peak Diode Recovery dv/dt Waveforms

■ TEST CIRCUITS AND WAVEFORMS (Cont.)

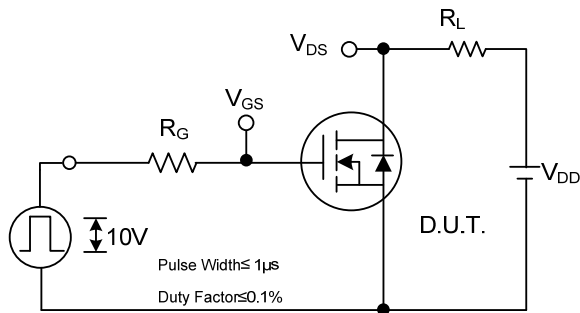


Fig. 2A Switching Test Circuit

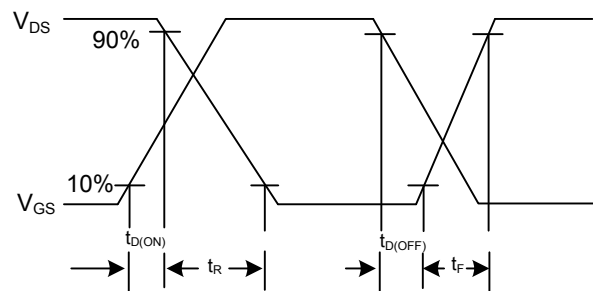


Fig. 2B Switching Waveforms

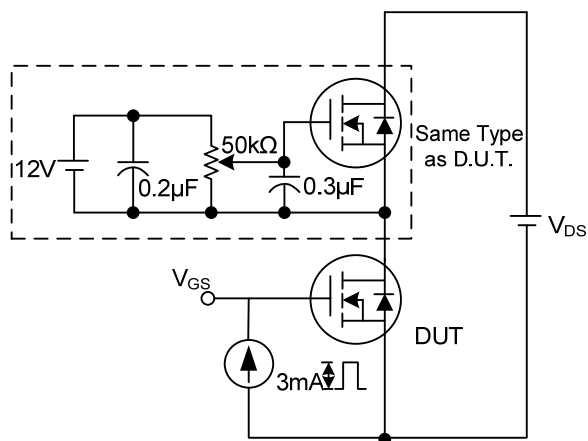


Fig. 3A Gate Charge Test Circuit

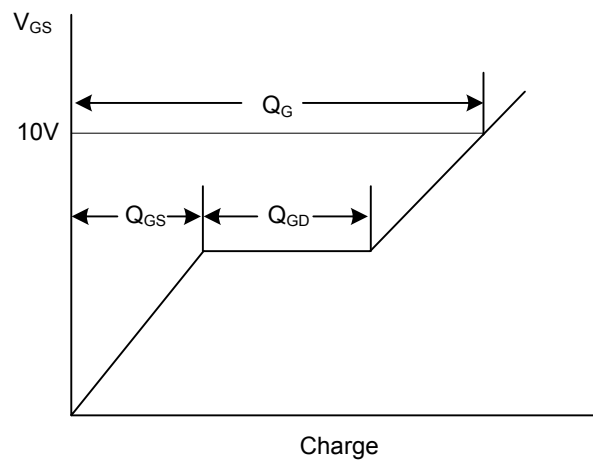


Fig. 3B Gate Charge Waveform

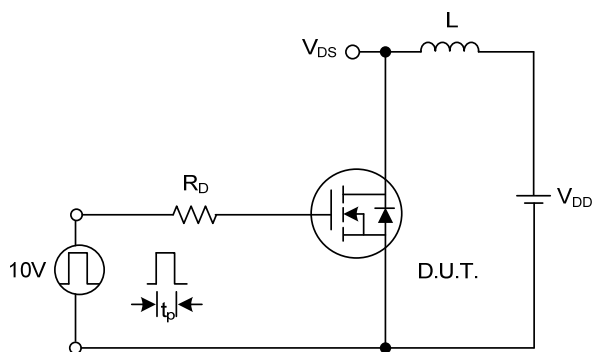


Fig. 4A Unclamped Inductive Switching Test Circuit

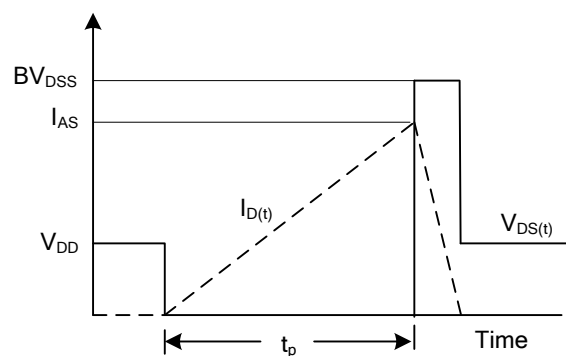


Fig. 4B Unclamped Inductive Switching Waveforms

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