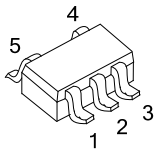
U74CBT1G125

CMOS IC

SINGLE FET BUS SWITCH



SOT-353

■ DESCRIPTION

The **U74CBT1G125** features a single high-speed line switch. The switch is disabled when the output-enable ($\overline{OE}$) input is high.

■ FEATURES

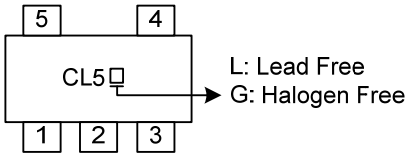
* 5Ω Switch Connection Between Two Ports
* Inputs are TTL-Voltage compatible

■ ORDERING INFORMATION

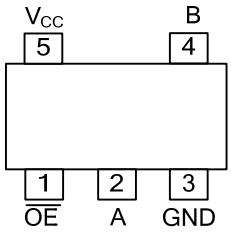
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74CBT1G125L-AL5-R	U74CBT1G125G-AL5-R	SOT-353	Tape Reel

U74CBT1G125G-AL5-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) AL5: SOT-353 (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



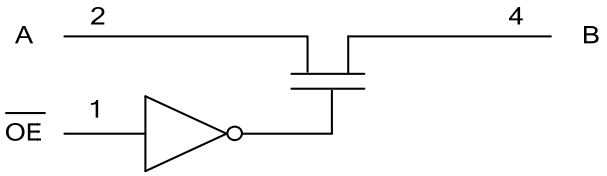
■ PIN CONFIGURATION



■ FUNCTION TABLE (each gate)

INPUT $\overline{OE}$	OUTPUT
L	A port = B port
H	Disconnect

■ LOGIC DIAGRAM (positive logic)



■ ABSOLUTE MAXIMUM RATING (Unless otherwise specified) (Note 1)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ 7	V
Input Voltage	V_I	-0.5 ~ 7	V
Continuous channel current		128	mA
Input Clamp Current(V_I<0)	I_{IK}	-50	mA
Storage Temperature	T_{STG}	-65 ~ +150	°C

Notes: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

■ RECOMMENDED OPERATING COMDITIONS (Unless otherwise specified)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	4		5.5	V
High-control input voltage	V_{IH}	2			V
Low-control input voltage	V_{IL}			0.8	V
Operating Temperature	T_A	-40		+125	°C

■ STATIC CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Digital Input Diode Voltage	V_{IK}	V_{CC} =4.5V, I_I=-18mA				-1.2	V
Input Leakage Current	I_I	V_{CC} =5.5V, V_I=V_{CC} or GND				±1	μA
V_{CC} or GND Current	I_{CC}	V_{CC} = 5.5V, V_I=5.5V or GND, I_O=0				1	μA
Control input	C_I	V_O=3V or 0			3		pF
I/O Capacitance (OFF)	C_{IO}	V_O=3V or 0, $\overline{OE}$ = V_{CC}			4		pF
Resistor between two ports	R_{ON}	V_{CC} =4V, TYP at V_{CC} =4V, V_I=2.4V, I_I=15mA			14	20	Ω
		V_{CC} =4.5V, V_I=0V	I_I=64mA		5	7	Ω
			I_I=30mA		5	7	Ω
		V_{CC} =4.5V, V_I=2.4V, I_I=15mA			10	15	Ω

■ DYNAMIC CHARACTERISTICS

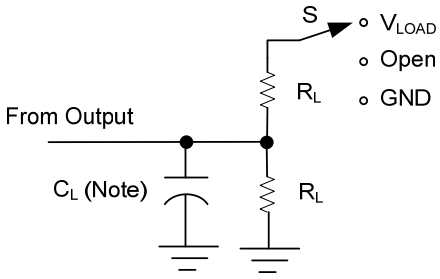
(Input: t_R, t_F≤2.5ns; PRR≤10MHz; C_L=50pF, unless otherwise specified)

See Fig. 1 and Fig. 2 for test circuit and waveforms.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
From input (A or B) to output (B or A) (Note)	t_{pd}	V_{CC}=4V, C_L=50pF, R_L=500Ω			0.35	ns
		V_{CC}= 5V±0.5V, C_L=50pF, R_L=500Ω			0.25	ns
From input $\overline{OE}$ to output (A or B)	t_{en}	V_{CC}=4V, C_L=50pF, R_L=500Ω			5.5	ns
		V_{CC}= 5V±0.5V, C_L=50pF, R_L=500Ω	1.6		4.9	ns
From input $\overline{OE}$ to output (A or B)	t_{dis}	V_{CC}=4V, C_L=50pF, R_L=500Ω			4.5	ns
		V_{CC}= 5V±0.5V, C_L=50pF, R_L=500Ω	1.0		4.2	ns

Notes: 1. t_{pd}: t_{PLH} and t_{PHL}.
2. t_{en}: t_{PZL} and t_{PZH}.
3. t_{dis}: t_{PLZ} and t_{PHZ}.

■ TEST CIRCUIT AND WAVEFORMS (C_L=50pF, R_L=500Ω, V_{LOAD}=7V, V_M=1.5V)



TEST	S
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}

Note: C_L includes probe and jig capacitance.

Fig. 1 Load circuitry for switching times.

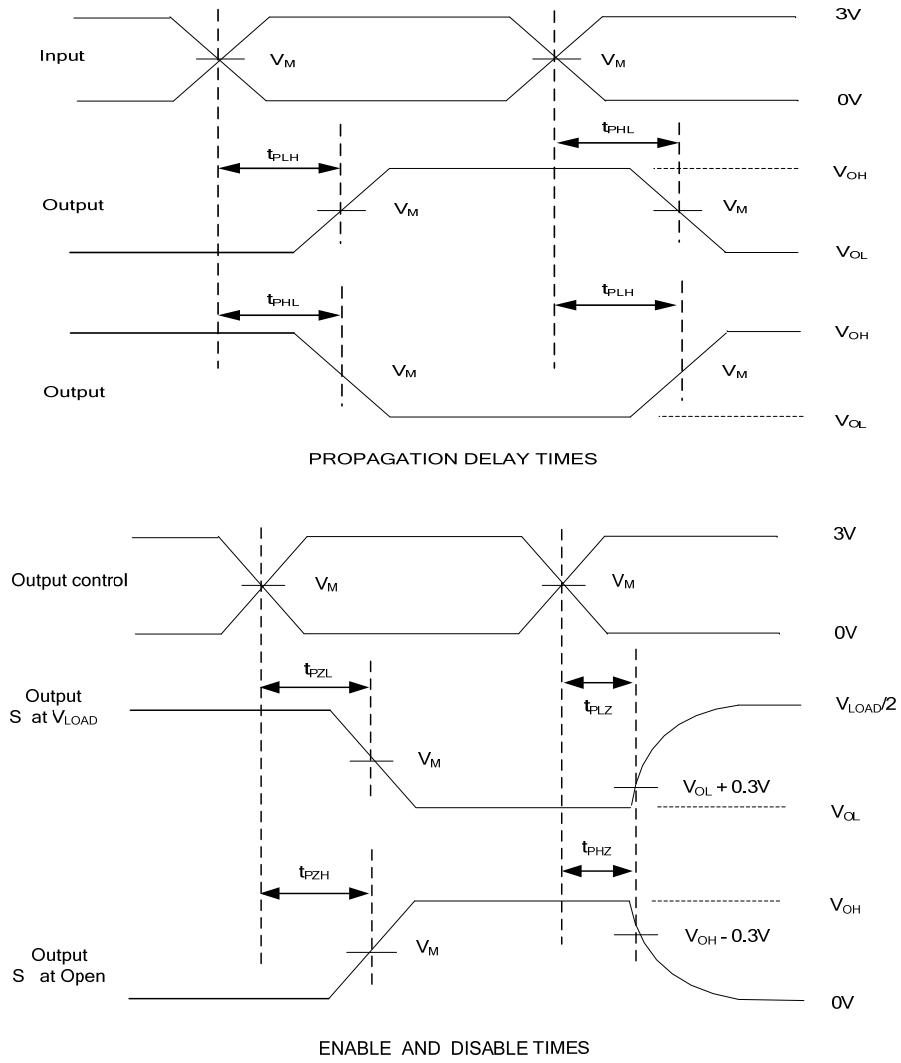


Fig. 2 Propagation delay from input(A) to output(B) and Output transition time.