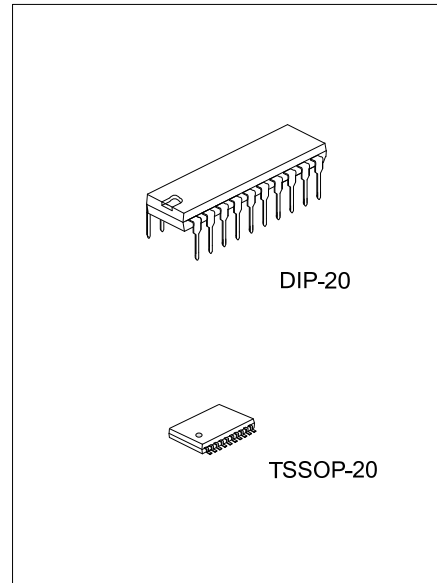




U74HCT374

CMOS IC

OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS



DESCRIPTION

The **U74HCT374** is a octal edge-triggered D-type flip-flops with 3-state outputs and it has 8 channels.

When the \overline{OE} input is low, on the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels of the data (D) inputs.

When the \overline{OE} input is high, the outputs are in the high-impedance.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FEATURES

- * Inputs are TTL-Voltage Compatible
- * Operate from 4.5V to 5.5V
- * Inputs Accept Voltages to 5.5V
- * Max t_{pd} of 25ns at $V_{CC}=5.5V$, $C_L=50pF$
- * Typ $V_{OL} < 0.26V$ at $V_{CC}=4.5V$, $I_{OL}=6mA$, $T_A=25^\circ C$
- * Typ $V_{OH} > 3.98V$ at $V_{CC}=4.5V$, $I_{OH}=-6mA$, $T_A=25^\circ C$

ORDERING INFORMATION

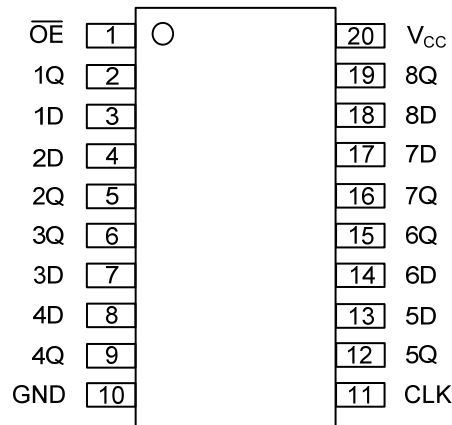
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74HCT374L-D20-T	U74HCT374G-D20-T	DIP-20	Tube
U74HCT374L-P20-R	U74HCT374G-P20-R	TSSOP-20	Tape Reel

<p>U74HCT374G-D20-T</p> <p>(1)Packing Type (2)Package Type (3)Green Package</p>	<p>(1) T: Tube, R: Tape Reel (2) D20: DIP-20, P20: TSSOP-20 (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING

DIP-20	TSSOP-20
<p>UTC □□□□ → Date Code L: Lead Free U74HCT374 □ → G: Halogen Free □□ → Lot Code</p>	<p>UTC □□□□ → Date Code L: Lead Free U74HCT374 □ → G: Halogen Free □□ → Lot Code</p>

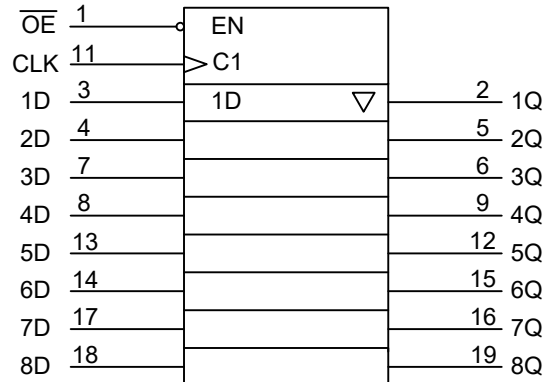
■ PIN CONFIGURATION



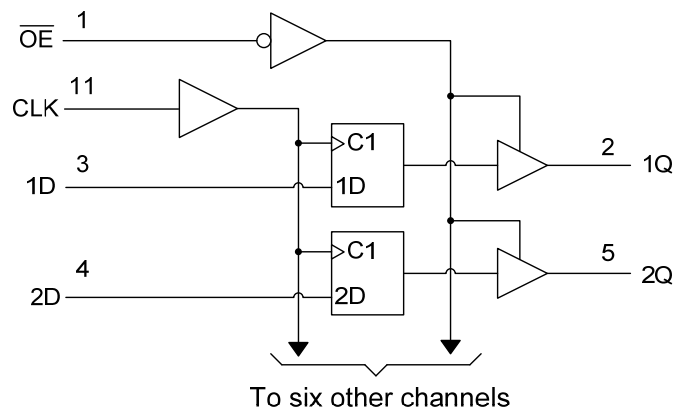
■ FUNCTION TABLE

INPUTS(\overline{OE})	INPUTS(CLK)	INPUTS(D)	OUTPUT(Q)
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

■ LOGIC SYMBOL



■ LOGIC DIAGRAM



■ ABSOLUTE MAXIMUM RATING (Unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ 7	V
Input Voltage	V_{IN}	-0.5 ~ 7	V
Output Voltage	V_{OUT}	-0.5 ~ $V_{CC} + 0.5$	V
V_{CC} or GND Current	I_{CC}	±70	mA
Output Current	I_{OUT}	±35	mA
Input Clamp Current	I_{IK}	-20	mA
Output Clamp Current	I_{OK}	±20	mA
Storage Temperature	T_{STG}	-65 ~ + 150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	4.5		5.5	V
High-Level Input Voltage	V_{IH}	2			V
Low-Level Input Voltage	V_{IL}			0.8	V
Input Voltage	V_{IN}	0		V_{CC}	V
Output Voltage	V_{OUT}	0		V_{CC}	V
Input Rise or Fall Times	t_R, t_F			500	ns/V
Operating free-air temperature	T_A	-40		+125	°C

■ ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Voltage High-Level	V_{OH}	$V_{CC}=4.5V, I_{OH}=-20\mu A$	4.4	4.499		V
		$V_{CC}=4.5V, I_{OH}=-6mA$	3.98	4.3		
Output Voltage Low-Level	V_{OL}	$V_{CC}=4.5V, I_{OL}=20\mu A$		0.001	0.1	V
		$V_{CC}=4.5V, I_{OL}=6mA$		0.17	0.26	
Input Leakage Current	$I_{I(LEAK)}$	$V_{CC}=5.5V, V_{IN}=0$ or $5.5V$		±0.1	±100	nA
Leakage Current (For output in high-impedance state)	I_{OZ}	$V_{CC}=5.5V, V_{IN}=V_{IH}$ or $V_{IH}, V_{OUT}=0$ or $5.5V$		±0.01	±0.5	µA
Quiescent Supply Current	I_{CC}	$V_{CC}=5.5V, V_{IN}=V_{CC}$ or $GND, I_{OUT}=0$			8	µA
Additional quiescent supply current	ΔI_{CC}	$V_{CC}=5.5V, \text{one input at } 0.5V \text{ or } 3.4V, \text{Other inputs at } V_{CC} \text{ or } GND$		1.4	2.4	mA
Input Capacitance	C_{IN}	$V_{CC}=4.5V$ to $5V$		3	10	pF

■ TIMING REQUIREMENTS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Clock Frequency	f_{CLOCK}	$V_{CC}=4.5V$			31	MHz
		$V_{CC}=5.5V$			36	
Pulse Width, CLK High or Low	t_W	$V_{CC}=4.5V$	16			ns
		$V_{CC}=5.5V$	14			
Setup Time, Data Before CLK↑	t_{SU}	$V_{CC}=4.5V$	20			ns
		$V_{CC}=5.5V$	17			
Hold Time, Data After CLK↑	t_H	$V_{CC}=4.5V$	10			ns
		$V_{CC}=5.5V$	10			

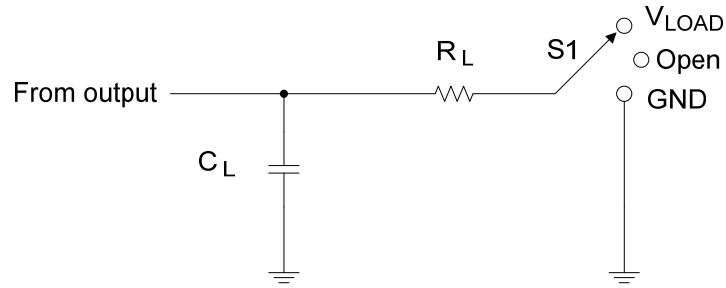
■ SWITCHING CHARACTERISTICS (See TEST CIRCUIT AND WAVEFORMS)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum Clock Frequency	$f_{(MAX)}$	$V_{CC}=4.5V, C_L=50pF$	31	36		MHz
		$V_{CC}=5.5V, C_L=50pF$	36	40		
From CLK to Q	t_{PD} (t_{PLH}/t_{PHL})	$V_{CC}=4.5V, C_L=50pF$		30	36	ns
		$V_{CC}=5.5V, C_L=50pF$		25	32	
		$V_{CC}=4.5V, C_L=150pF$		40	46	
		$V_{CC}=5.5V, C_L=150pF$		35	41	
From \overline{OE} to Q	t_{EN} (t_{PZL}/t_{PZH})	$V_{CC}=4.5V, C_L=50pF$		26	30	ns
		$V_{CC}=5.5V, C_L=50pF$		23	27	
		$V_{CC}=4.5V, C_L=150pF$		34	40	
		$V_{CC}=5.5V, C_L=150pF$		29	36	
From \overline{OE} to Q	t_{DIS} (t_{PLZ}/t_{PHZ})	$V_{CC}=4.5V, C_L=50pF$		23	30	ns
		$V_{CC}=5.5V, C_L=50pF$		22	27	
Output transition rise/fall time	t_T (t_R/t_F)	$V_{CC}=4.5V, C_L=50pF$		10	12	ns
		$V_{CC}=5.5V, C_L=50pF$		9	11	
		$V_{CC}=4.5V, C_L=150pF$		18	42	
		$V_{CC}=5.5V, C_L=150pF$		16	38	

■ OPERATING CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNIT
Power Dissipation Capacitance	C_{PD}	No load, $V_{CC}=5V, f=1MHz$	85	pF

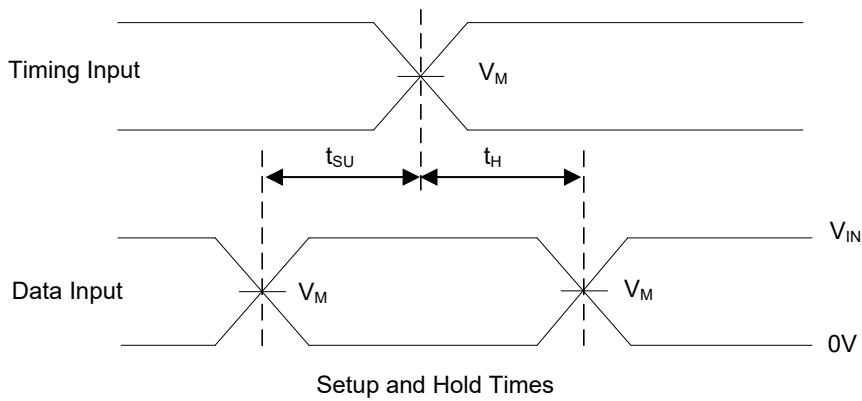
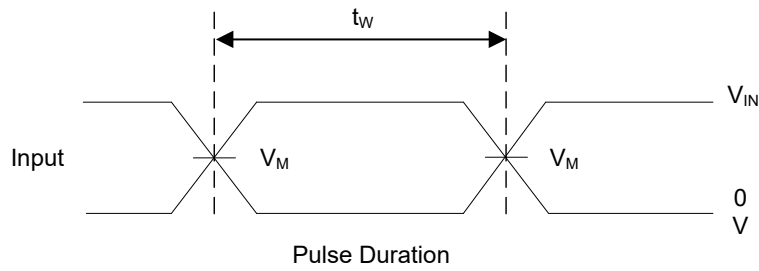
■ TEST CIRCUIT AND WAVEFORMS



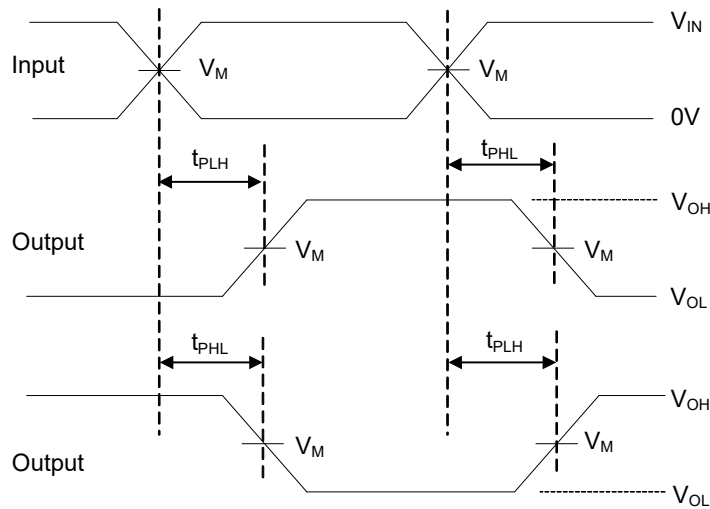
Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

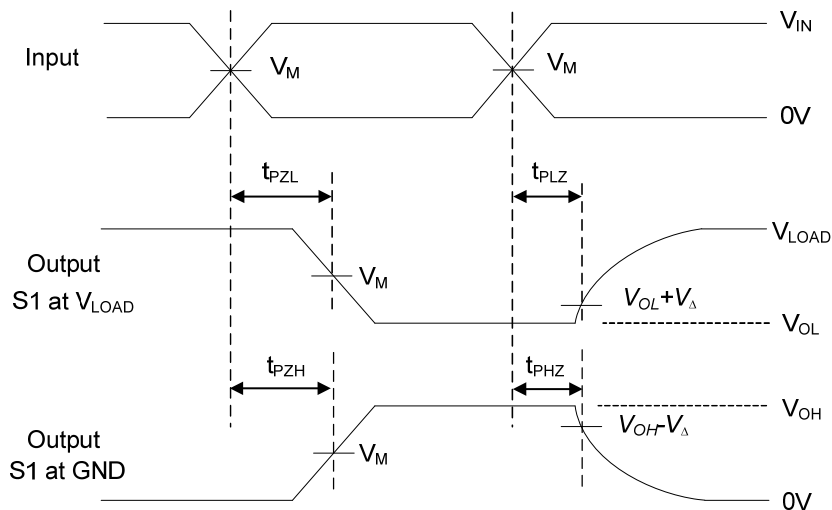
V_{CC}	Input		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_{IN}	t_R, t_F					
$5V \pm 0.5V$	V_{CC}	$\leq 3ns$	$V_{CC}/2$	V_{CC}	15pF	1k Ω	0.5V
					50pF		



■ TEST CIRCUIT AND WAVEFORMS(Cont.)



Voltage Waveforms Propagation Delay Times



Voltage Waveforms Enable and Disable Times

Note: A. C_L includes probe and jig capacitance.

B. $P_{RR} \leq 1\text{MHz}$, $Z_O = 50\Omega$, $t_R \leq 3\text{ns}$, $t_F \leq 3\text{ns}$.

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