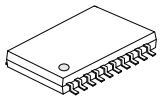
U74LVC640

CMOS IC

OCTAL BUS TRANSCEIVER WITH 3-STATE INVERTING OUTPUTS



TSSOP-20

■ DESCRIPTION

The **U74LVC640** is designed for asynchronous communication between data buses and has inverting outputs. While the direction-control(DIR) input is high, data transmits from the A bus to the B bus. In contrast, Data transmits from the B bus to the A bus DIR input is low. The output-enable($\overline{OE}$) will disable the device and isolate from the buses when high voltage is applied on it.

■ FEATURES

* Supply Voltage Range From 1.2V to 3.6V
* Input Accept Voltages up to 5.5V
* Partial-Power-Down Mode Operation
* Max t_{PD} is 6.3ns at 3.3V

■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74LVC640L-P20-R	U74LVC640G-P20-R	TSSOP-20	Tape Reel

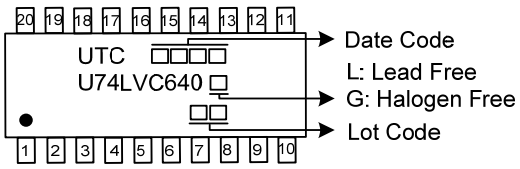
U74LVC640G-P20-R

(1)Packing Type — (1) R: Tape Reel

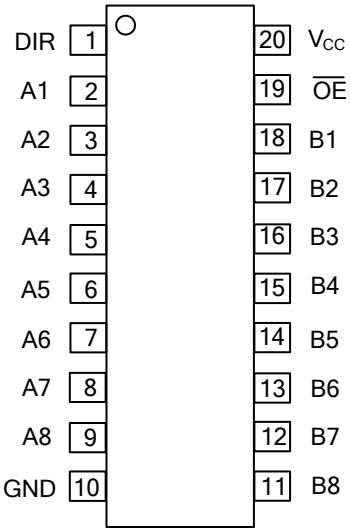
(2)Package Type — (2) P20: TSSOP-20

(3)Green Package — (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



■ PIN CONFIGURATION

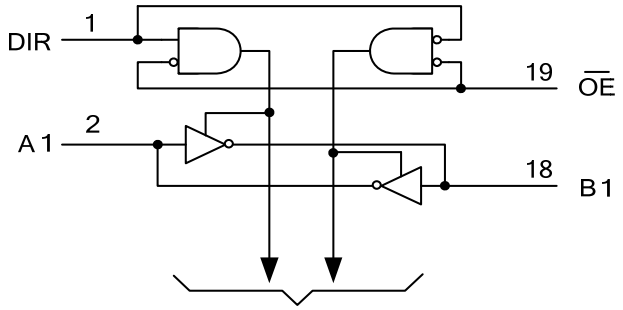


■ FUNCTION TABLE

INPUT		FUNCTION
$\overline{OE}$	DIR	
H	X	Isolation
L	H	Transmit data from A bus to B bus, B=A
L	L	Transmit data from B bus to A bus, A=B

Note: H: HIGH voltage level L: LOW voltage level X: Don't care

■ LOGIC DIAGRAM (Negative Logic)



Seven Other channels

■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ 6.5	V
Input Voltage	V_{IN}	-0.5 ~ 6.5	V
Voltage Applied To Output In High-Impedance Or Power-Off State	V_{OUT}	-0.5 ~ 6.5	V
Voltage applied to output in high or low state		-0.5 ~ V_{CC}+0.5	
Input Clamp Current	I_{IK}	-50	mA
Output Clamp Current	I_{OK}	-50	mA
Output Current	I_{OUT}	±50	mA
V_{CC} or GND Current	I_{CC}	±100	mA
Storage Temperature	T_{STG}	-65 ~ +150	˚C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ OPERATING CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS		TYP	UNIT
Power Dissipation Capacitance Per Transceiver	C_{PD}	$\overline{OE}$ =0 f=10MHZ	V_{CC}=1.8V	42	pF
			V_{CC}=2.5V	43	
			V_{CC}=3.3V	45	
		$\overline{OE}$ =1 f=10MHZ	V_{CC}=1.8V	1	
			V_{CC}=2.5V	1	
			V_{CC}=3.3V	2	

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	Min	TYP	Max	UNIT
Supply Voltage	V_{CC}	Operating	1.65		3.6	V
		Data retention only	1.5			
High-Level Input Voltage	V_{IH}	V_{CC}=1.65V~1.95V	0.65× V_{CC}			V
		V_{CC}=2.3V~2.7V	1.7			
		V_{CC}=2.7V~3.6V	2			
Low-Level Input Voltage	V_{IL}	V_{CC}=1.65V~1.95V			0.35× V_{CC}	V
		V_{CC}=2.3V~2.7V			0.7	
		V_{CC}=2.7V~3.6V			0.8	
Input Voltage	V_{IN}		0		5.5	V
Output Voltage	V_{OUT}		0		Vcc	V
Output High Current	I_{OH}	V_{CC}=1.65V			-4	mA
		V_{CC}=2.3V			-8	
		V_{CC}=2.7V			-12	
		V_{CC}=3V			-24	
Output Low Current	I_{OL}	V_{CC}=1.65V			4	mA
		V_{CC}=2.3V			8	
		V_{CC}=2.7V			12	
		V_{CC}=3V			24	

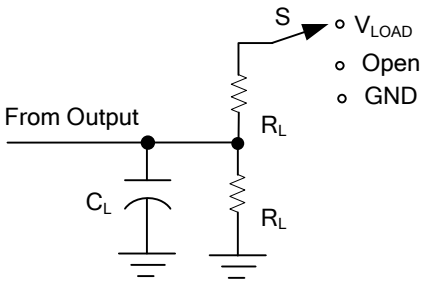
■ ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	Min	TYP	Max	UNIT
High-Level Output Voltage	V_{OH}	I_{OH}=–100μA, V_{CC}=1.65V~3.6V	V_{CC}-0.2			V
		I_{OH}=–4mA, V_{CC}=1.65V	1.29			
		I_{OH}=–8mA, V_{CC}=2.3V	1.9			
		I_{OH}=–12mA, V_{CC}=2.7V	2.2			
		I_{OH}=–12mA, V_{CC}=3V	2.4			
		I_{OH}=–24mA, V_{CC}=3V	2.3			
Low-Level Output Voltage	V_{OL}	I_{OL}=100μA, V_{CC}=1.65V~3.6V			0.1	V
		I_{OL}=4mA, V_{CC}=1.65V			0.24	
		I_{OL}=8mA, V_{CC}=2.3V			0.3	
		I_{OL}=12mA, V_{CC}=2.7V			0.4	
		I_{OL}=24mA, V_{CC}=3V			0.55	
Input Current	$I_{I(LEAK)}$	V_{IN}=5.5V or GND, V_{CC}=3.6V			±1	μA
Power OFF Leakage Current	I_{OFF}	V_{IN}=5.5V or GND, V_{CC}=0V			±1	μA
Output Off-State Current	I_{OZ}	V_{OUT}=0~5.5V, V_{CC}=3.6V			±1	μA
Quiescent Supply Current	I_Q	V_{IN}=V_{CC} or GND, I_{OUT}=0, V_{CC}=3.6V			1	μA
		V_{IN}=3.6~5.5v, I_{OUT}=0, V_{CC}=3.6V			1	μA
Additional Quiescent Current Per Input Pin	ΔI_Q	V_{CC}=2.7V~3.6V, V_{IN}=V_{CC} -0.6V, I_{OUT}=0			500	μA

■ SWITCHING CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	Min	TYP	Max	UNIT
Propagation Delay (From A to B Or From B to A)	t_{PLH} / t_{PHL}	V_{CC} =1.8 V ± 0.15 V	1	6	12.2	ns
		V_{CC} =2.5 V ± 0.2 V	1	3.9	7.8	
		V_{CC} =2.7 V	1	4.2	7.1	
		V_{CC} =3.3 V ± 0.3 V	1.5	3.8	6.1	
3-State Output Enable Time (From $\overline{OE}$ to A or B)	t_{PZH} / t_{PZL}	V_{CC} =1.8 V ± 0.15 V	1	7	14.8	ns
		V_{CC} =2.5 V ± 0.2 V	1	4.5	10	
		V_{CC} =2.7 V	1	5.4	9.3	
		V_{CC} =3.3 V ± 0.3 V	1.5	4.4	8.3	
3-State Output Disable Time (From $\overline{OE}$ A to A or B)	t_{PLZ} / t_{PLH}	V_{CC} =1.8 V ± 0.15 V	1	7.8	16.5	ns
		V_{CC} =2.5 V ± 0.2 V	1	4	9	
		V_{CC} =2.7 V	1	4.4	8.3	
		V_{CC} =3.3 V ± 0.3 V	1.7	4.1	7.3	

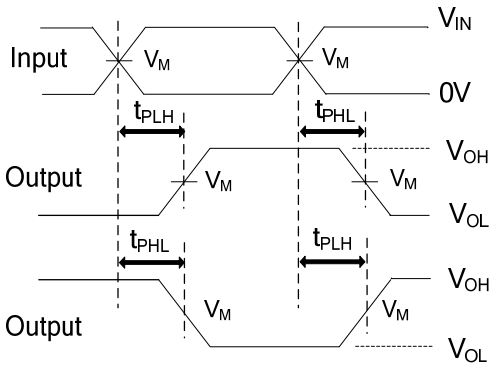
■ TEST CIRCUIT AND WAVEFORMS



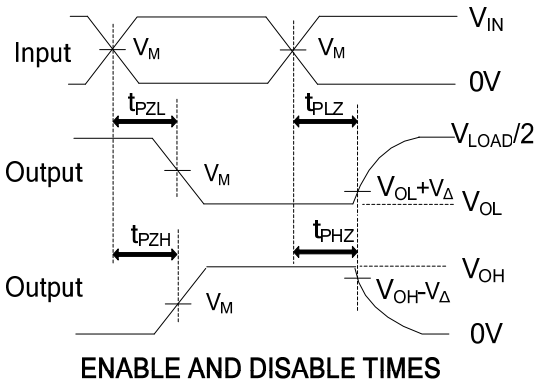
TEST	S
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	V_{LOAD}

TEST CIRCUIT

V_{CC}	INPUTS		V_M	V_Δ	C_L	R_L	V_{LOAD}
	V_{IN}	t_R/t_F					
1.8V ±0.15V	V_{CC}	≤2ns	$V_{CC}/2$	0.15V	30 pF	1 kΩ	2 x V_{CC}
2.5V ±0.2V	V_{CC}	≤2ns	$V_{CC}/2$	0.15V	30 pF	500Ω	2 x V_{CC}
2.7 V	2.7 V	≤2.5ns	1.5V	0.3V	50 pF	500Ω	6V
3.3V ±0.3V	2.7 V	≤2.5ns	1.5V	0.3V	50 pF	500Ω	6V



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

Note: C_L includes probe and jig capacitance.
All input pulses are supplied by generators having the following characteristics: PRR ≤10MHz, Zo = 50Ω.