

U74HCT125

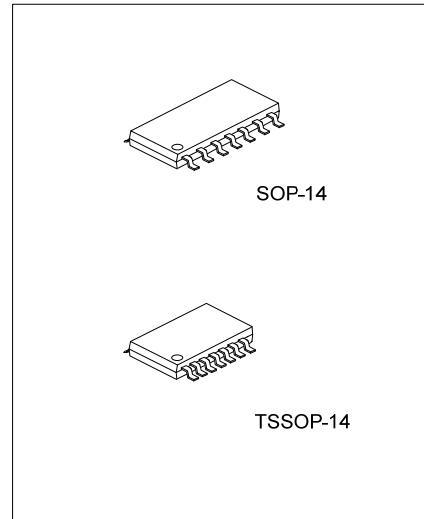
CMOS IC

QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

■ DESCRIPTION

The **U74HCT125** is a quadruple bus buffer gates with 3-state output. When \overline{OE} is high, the Y outputs are in a high-impedance state. When \overline{OE} is low, the device passes noninverted data from the A input to the Y output.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.



■ FEATURES

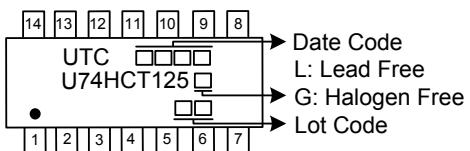
- * TTL-Voltage Compatible
- * Max t_{PD} of 12 ns from A to Y at 5.5 V, $C_L = 50 \text{ pF}$
- * Low power consumption, $I_{CC} = 8\mu\text{A}$ (Max) at 5.5V
- * $\pm 6\text{mA}$ output driver at 5V

■ ORDERING INFORMATION

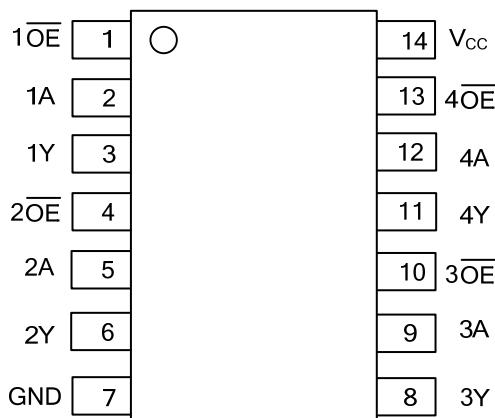
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74HCT125L-S14-R	U74HCT125G-S14-R	SOP-14	Tape Reel
U74HCT125L-P14-R	U74HCT125G-P14-R	TSSOP-14	Tape Reel

U74HCT125G-S14-R 	(1)R: Tape Reel (2)S14: SOP-14, P14: TSSOP-14 (3)G: Halogen Free and Lead Free, L: Lead Free
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■ MARKING



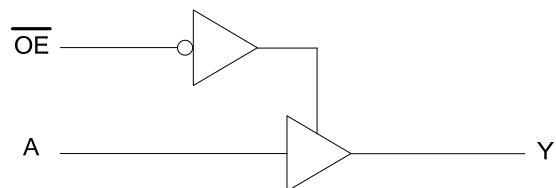
■ PIN CONFIGURATION



■ FUNCTION TABLE (each buffer)

INPUTS		OUTPUTS
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z

■ LOGIC DIAGRAM (each buffer)



■ ABSOLUTE MAXIMUM RATING (unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V _{CC}	-0.5~7	V
Input Voltage	V _{IN}	-0.5~7	V
Output Voltage	V _{OUT}	-0.5~V _{CC} +0.5	V
Input Clamp Current (V _{IN} <0, or V _{IN} >0)	I _{IK}	±20	mA
Output Clamp Current (V _{OUT} <0, or V _{OUT} >V _{CC})	I _{OK}	±20	mA
Output Current	I _{OUT}	±35	mA
V _{CC} or GND Current	I _{CC}	±70	mA
Storage Temperature	T _{STG}	-65 ~ +150	°C

Note: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage	V _{CC}	4.5	5	5.5	V
High-Level Input Voltage (V _{CC} =4.5V to 5.5V)	V _{IH}	2			V
Low-Level Input Voltage (V _{CC} = 4.5V to 5.5V)	V _{IL}			0.8	V
Input Voltage	V _{IN}	0		V _{CC}	V
Output Voltage	V _{OUT}	0		V _{CC}	V
Input Transition Rise or Fall Rate	Δt/ΔV			500	ns/V
Operating Temperature	T _A	-40	25	85	°C

■ ELECTRICAL CHARACTERISTICS (T_A =25°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Output Voltage	V _{OH}	I _{OH} = -20μA, V _{CC} =4.5 V	4.4	4.5		V
		I _{OH} = -6 mA, V _{CC} =4.5 V	3.98	4.3		
Low-Level Output Voltage	V _{OL}	I _{OL} = 20 μA, V _{CC} =4.5 V		0.001	0.1	V
		I _{OL} = 6 mA , V _{CC} =4.5 V		0.17	0.26	
Input Leakage Current (A or OE input)	I _{I(LEAK)}	V _{IN} = 5.5V or GND, V _{CC} =5.5 V		±0.1	±100	μA
High-Impedance State Current	I _{OZ}	V _{OUT} = V _{CC} or GND, V _{CC} =5.5 V		±0.01	±0.5	μA
Quiescent Supply Current	I _{CC}	V _{IN} = V _{CC} or GND, I _{OUT} = 0, V _{CC} =5.5 V			8	μA
Additional Quiescent Supply Current	Δ I _{CC}	One input at 0.5V or 2.4V, V _{CC} =5.5 V, other inputs at V _{CC} or GND		1.4	2.4	mA
Input Capacitance	C _{IN}	V _{CC} =4.5V to 5.5 V		3	10	pF

■ SWITCHING CHARACTERISTICS

($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay from Input A to Output Y, t_{PD}	t_{PLH}/ t_{PHL}	$V_{CC} = 4.5 \text{ V}$		15	26	ns
		$V_{CC} = 5.5 \text{ V}$		12	23	
Propagation Delay from Input OE to Output Y, t_{EN}	t_{PZH}/ t_{PZL}	$V_{CC} = 4.5 \text{ V}$		18	28	ns
		$V_{CC} = 5.5 \text{ V}$		15	25	
Propagation delay from input OE to output Y, t_{DIS}	t_{PHZ}/ t_{PLZ}	$V_{CC} = 4.5 \text{ V}$		15	26	ns
		$V_{CC} = 5.5 \text{ V}$		13	23	
Output transition (rise and fall) time, t_T	t_{TLH}/ t_{THL}	$V_{CC} = 4.5 \text{ V}$		8	15	ns
		$V_{CC} = 5.5 \text{ V}$		7	14	

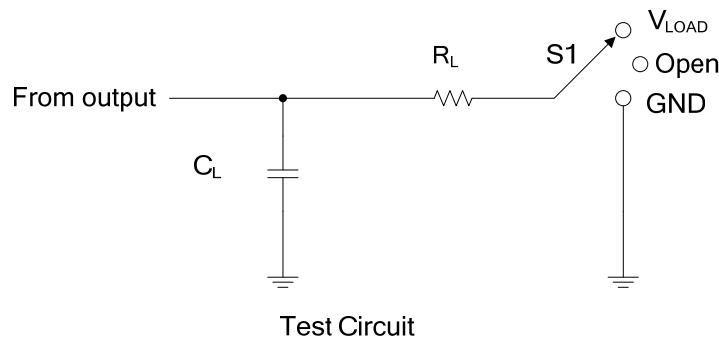
($C_L = 150 \text{ pF}$, $T_A = 25^\circ\text{C}$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay from Input A to Output Y, t_{PD}	t_{PLH}/ t_{PHL}	$V_{CC} = 4.5 \text{ V}$		19	36	ns
		$V_{CC} = 5.5 \text{ V}$		16	32	
Propagation Delay from Input OE to Output Y, t_{EN}	t_{PZH}/ t_{PZL}	$V_{CC} = 4.5 \text{ V}$		25	40	ns
		$V_{CC} = 5.5 \text{ V}$		21	35	
Output transition (rise and fall) time, t_T	t_{TLH}/ t_{THL}	$V_{CC} = 4.5 \text{ V}$		17	42	ns
		$V_{CC} = 5.5 \text{ V}$		14	38	

■ OPERATING CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

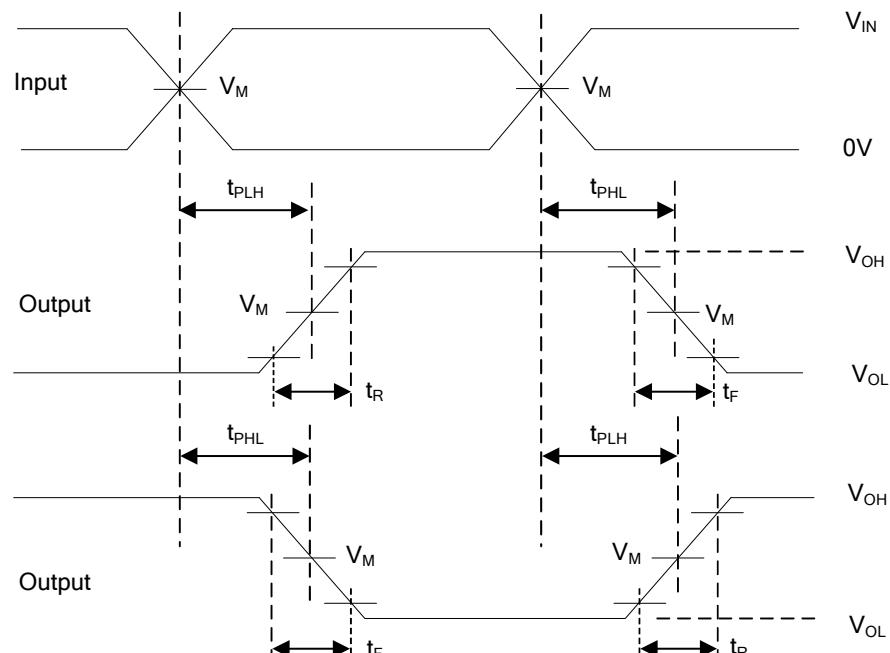
PARAMETER	SYMBOL	TEST CONDITIONS	TYP	UNIT
Power dissipation capacitance	C_{PD}		35	pF

■ TEST CIRCUIT AND WAVEFORMS



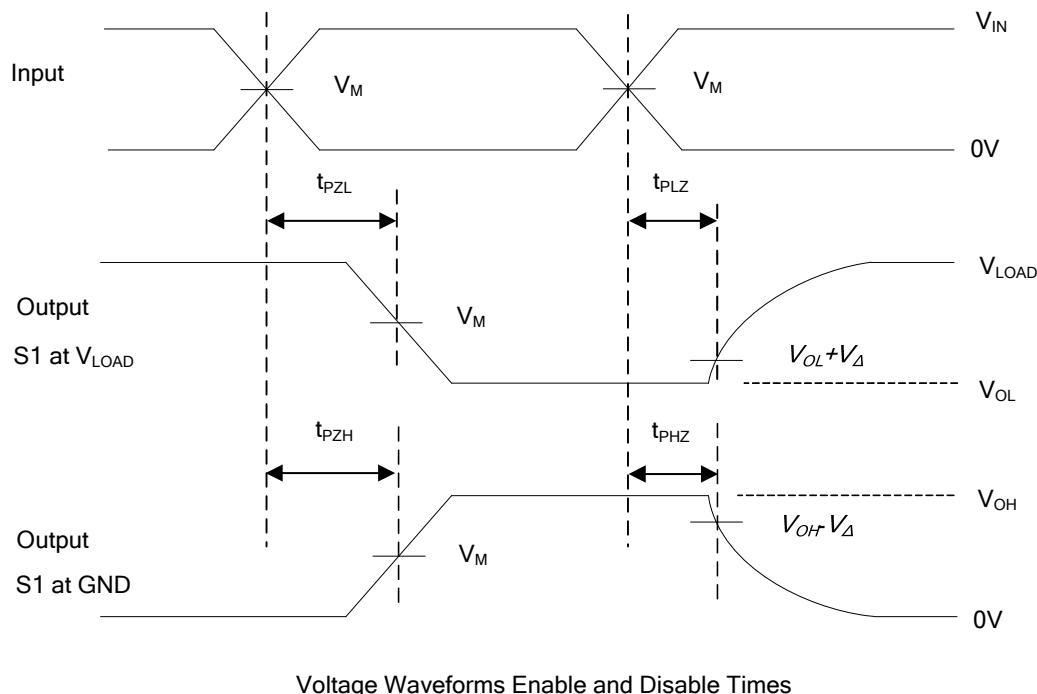
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	Input		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_{IN}	t_R, t_F					
$5V \pm 0.5V$	V_{CC}	$\leq 3ns$	$V_{CC}/2$	V_{CC}	50pF 150pF	1k Ω	0.5V



Voltage Waveforms Propagation Delay Times

■ TEST CIRCUIT AND WAVEFORMS (Cont.)



Voltage Waveforms Enable and Disable Times

Notes: 1. C_L includes probe and jig capacitance.

2. All input pulses are supplied by generators having the following characteristics: P_{RR} ≤ 1MHz, Z_O = 50Ω.

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