



12N06

Preliminary

Power MOSFET

**12 Amps, 60 Volts
N-CHANNEL POWER MOSFET**

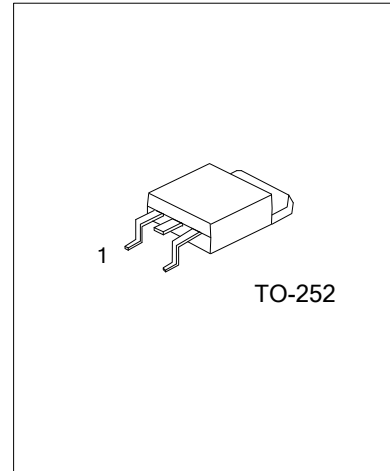
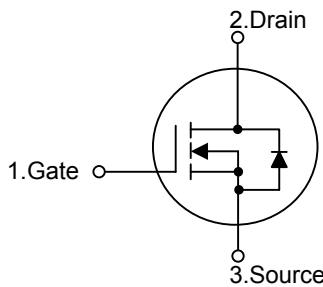
■ DESCRIPTION

The UTC **UT12N06** is an N-channel mode Power MOSFET using UTC's advanced technology to provide customers with minimum on-state resistance with extremely high dense cell design, rugged avalanche characteristics and less critical alignment steps .

■ FEATURES

- * $V_{DS(V)} = 60V$
- * $I_D = 12A$
- * $R_{DS(on)} < 0.10\Omega @ V_{GS} = 10 V$
 $R_{DS(on)} < 0.12\Omega @ V_{GS} = 5.0 V$
- * High switching speed
- * Low gate charge

■ SYMBOL



■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
12N06L-TN3-R	12N06G-TN3-R	TO-252	G	D	S	Tape Reel

<p>12N06L-TN3-R</p>	<p>(1) R: Tape Reel</p> <p>(2) TN3: TO-252</p> <p>(3) G: Halogen Free, L: Lead Free</p>
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■ ABSOLUTE MAXIMUM RATINGS($T_C = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT	
Drain-Source Voltage ($V_{GS}=0$)		V_{DSS}	60	V	
Drain-Gate Voltage ($R_{GS}=20\text{K}\Omega$)		V_{DGR}	60	V	
Gate-Source Voltage		V_{GSS}	± 20	V	
Drain Current	Continuous	I_D	$T_C = 25^\circ\text{C}$	12	A
			$T_C = 100^\circ\text{C}$	8.5	A
	Pulsed (Note 2)		I_{DM}	48	A
Power Dissipation		P_D	30	W	
Derating Factor			0.2	$\text{W}/^\circ\text{C}$	
Peak Diode Recovery dv/dt (Note 3)		dv/dt	15	V/ns	
Avalanche Energy (Note 4)		E_{AS}	100	mJ	
Junction Temperature		T_J	+150	$^\circ\text{C}$	
Storage Temperature		T_{STG}	-55~+150	$^\circ\text{C}$	

Note: 1 Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Pulse width limited by safe operating area
3. $I_{SD} \leq 12\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DS} \leq 40\text{V}$, $T_J \leq T_{JMAX}$
4. Starting $T_J = 25^\circ\text{C}$, $I_D = 6\text{A}$, $V_{DD} = 30\text{V}$

■ THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	100	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	5	$^\circ\text{C}/\text{W}$

■ ELECTRICAL CHARACTERISTICS (T_{CASE}=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage	BV _{DSS}	I _D =25mA, V _{GS} =0V	60			V	
Drain-Source Leakage Current	I _{DSS}	V _{DS} =Max rating, V _{GS} =0V			1	μA	
Gate- Source Leakage Current	Forward	V _{GS} =+20V, V _{DS} =0V			+100	nA	
	Reverse	V _{GS} =-20V, V _{DS} =0V			-100	nA	
ON CHARACTERISTICS							
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	1		3	V	
Static Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =6A		0.08	0.10	Ω	
		V _{GS} =5V, I _D =6A		0.10	0.12	Ω	
DYNAMIC PARAMETERS							
Input Capacitance	C _{ISS}	V _{GS} =0V, V _{DS} =25V, f=1.0MHz		350		pF	
Output Capacitance	C _{OSS}			75		pF	
Reverse Transfer Capacitance	C _{RSS}			30		pF	
SWITCHING PARAMETERS (Note 1,2)							
Total Gate Charge	Q _G	V _{GS} =5V, V _{DD} =48V, I _D =12A		7.5	10	nC	
Gate to Source Charge	Q _{GS}			2.5		nC	
Gate to Drain Charge	Q _{GD}			3.0		nC	
Turn-ON Delay Time	t _{D(ON)}	V _{DD} =30V, I _D =6A, R _G =4.7Ω, V _{GS} =4.5V (Figure 1.)		10		ns	
Rise Time	t _R			35		ns	
Turn-OFF Delay Time	t _{D(OFF)}			20		ns	
Fall-Time	t _F			13		ns	
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current	I _S				12	A	
Maximum Body-Diode Pulsed Current	I _{SM}				48	A	
Drain-Source Diode Forward Voltage (Note 1)	V _{SD}	I _S =12A, V _{GS} =0V			1.5	V	
Body Diode Reverse Recovery Time	t _{RR}	I _S =12A, V _{DD} =16V, di/dt=100A/μs T _J =150°C (Figure 3.)		50		ns	
Body Diode Reverse Recovery Charge	Q _{RR}				65		μC
Body Diode Reverse Recovery Current	I _{RRM}				2.5		A

- Notes: 1. Pulsed: pulse duration=300μs, duty cycle 1.5%
2. Essentially independent of operating temperature

■ TEST CIRCUITS AND WAVEFORMS

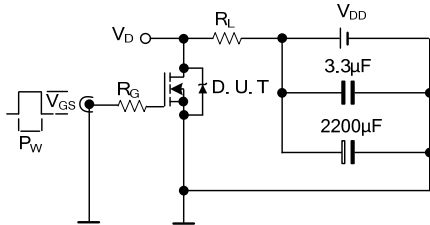


Figure 1. Switching Times Test Circuit for Resistive Load

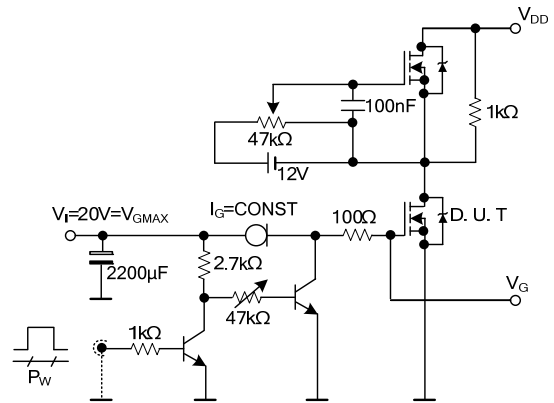


Figure 2. Gate Charge Test Circuit

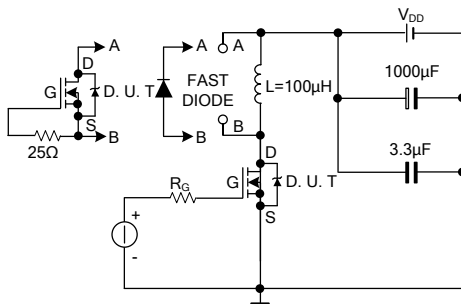


Figure 3. Test Circuit for Inductive Load Switching and Diode Recovery Times

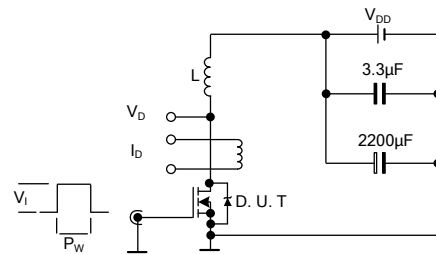


Figure 4. Unclamped Inductive Load Test Circuit

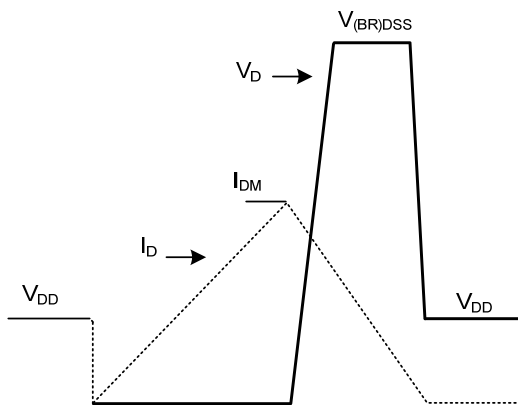


Figure 5. Unclamped Inductive Waveform

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