

6N10**Power MOSFET****6.5A, 100V N-CHANNEL
POWER MOSFET****■ DESCRIPTION**

The UTC **6N10** is an N-Channel enhancement mode power FET providing customers with excellent switching performance and minimum on-state resistance.

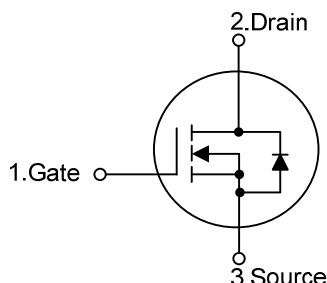
The UTC **6N10** is generally applied in voltage applications, such as DC motor control, audio amplifier and high efficiency switching DC/DC converters.

■ FEATURES

- * $R_{DS(ON)} \leq 0.2 \Omega$ @ $V_{GS}=10V$, $I_D=3.0A$

- * Fast switching

- * Improved dv/dt capability

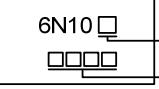
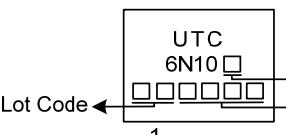
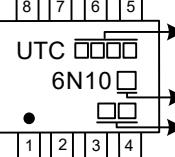
■ SYMBOL**■ ORDERING INFORMATION**

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
6N10L-AA3-R	6N10G-AA3-R	SOT-223	G	D	S	-	-	-	-	-	Tape Reel
6N10L-TM3-T	6N10G-TM3-T	TO-251	G	D	S	-	-	-	-	-	Tube
6N10L-TN3-R	6N10G-TN3-R	TO-252	G	D	S	-	-	-	-	-	Tape Reel
6N10L-TND-R	6N10G-TND-R	TO-252D	G	D	S	-	-	-	-	-	Tape Reel
6N10L-S08-R	6N10G-S08-R	SOP-8	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

6N10G-AA3-R	(1)Packing Type	(1) R: Tape Reel, T: Tube
	(2)Package Type	(2) AA3: SOT-223, TM3: TO-251, TN3: TO-252, TND: TO-252D, S08: SOP-8
	(3)Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING

PACKAGE	MARKING
SOT-223	 <p>L: Lead Free G: Halogen Free Date Code</p> <p>1</p>
TO-251 TO-252 TO-252D	 <p>Lot Code ←</p> <p>UTC 6N10</p> <p>L: Lead Free G: Halogen Free Date Code</p> <p>1</p>
SOP-8	 <p>Date Code</p> <p>UTC 6N10</p> <p>L: Lead Free G: Halogen Free</p> <p>Lot Code</p> <p>1 2 3 4</p>

■ ABSOLUTE MAXIMUM RATINGS ($T_c = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	Continuous	I_D	6.5	A
	Pulsed	I_{DM}	8.0	A
Repetitive Avalanche Energy (Duty Cycle $\leq 1\%$)	$L=0.1\text{mH}$	E_{AR}	1.25	mJ
Power Dissipation	SOT-223	P_D	2.2	W
	TO-251/TO-252		30	W
	TO-252D		1.6	W
	SOP-8		+150	°C
Junction Temperature		T_J	-55 ~ +150	°C
Storage Temperature		T_{STG}		

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.
Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	SOT-223	θ_{JA}	140	°C/W
	TO-251/TO-252		110	°C/W
	TO-252D		50	°C/W
	SOP-8		56.8	°C/W
Junction to Case	TO-251/TO-252	θ_{JC}	4.16	°C/W
	TO-252D		78	°C/W
	SOP-8			

Note: θ_{JA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.

θ_{JC} is guaranteed by design while θ_{JA} is determined by the user's board design.

■ ELECTRICAL CHARACTERISTICS ($T_J=25^\circ\text{C}$, unless otherwise noted)

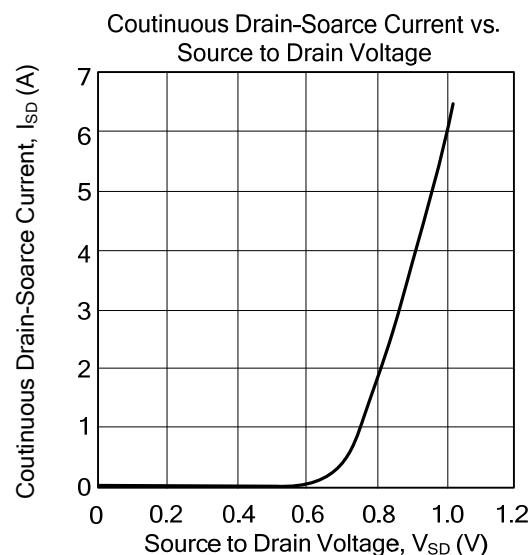
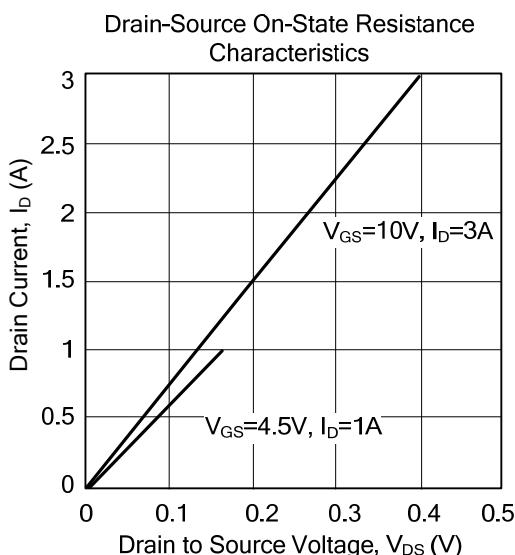
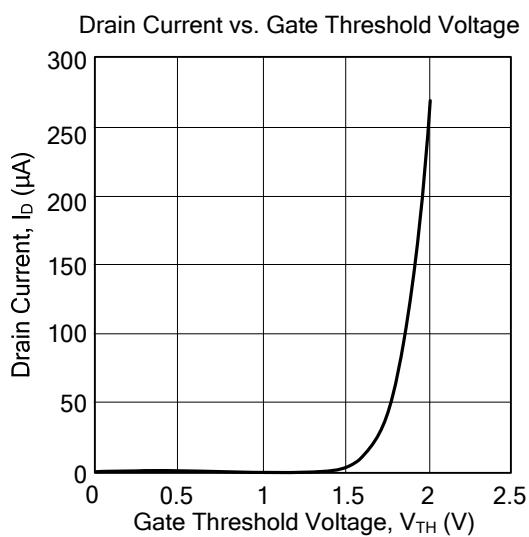
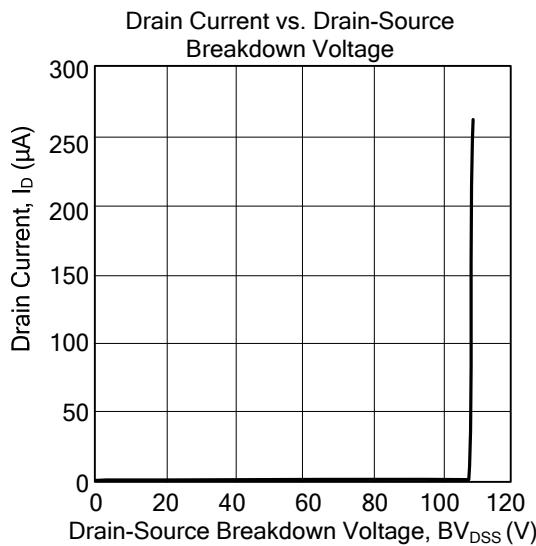
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=250\mu\text{A}, V_{GS}=0\text{V}$	100			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=100\text{V}, V_{GS}=0\text{V}$			1	μA
		$V_{DS}=100\text{V}, V_{GS}=0\text{V}, T_J=125^\circ\text{C}$			50	μA
		$V_{DS}=100\text{V}, V_{GS}=0\text{V}, T_J=150^\circ\text{C}$			250	μA
Gate- Source Leakage Current	Forward	$V_{GS}=+20\text{V}, V_{DS}=0\text{V}$			+100	nA
	Reverse	$V_{GS}=-20\text{V}, V_{DS}=0\text{V}$			-100	nA
On-State Drain Current (Note 2)	$I_{D(\text{on})}$	$V_{DS}=5.0\text{V}, V_{GS}=10\text{V}$	8.0			A
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(\text{TH})}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	1.0		3.0	V
Static Drain-Source On-State Resistance (Note 2)	$R_{DS(\text{ON})}$	$V_{GS}=10\text{V}, I_D=3\text{A}$		0.150	0.200	Ω
		$V_{GS}=10\text{V}, I_D=3\text{A}, T_J=125^\circ\text{C}$			0.350	Ω
		$V_{GS}=10\text{V}, I_D=3\text{A}, T_J=150^\circ\text{C}$			0.450	Ω
		$V_{GS}=4.5\text{V}, I_D=1.0\text{A}$		0.160	0.225	Ω
Forward Transconductance (Note 2)	g_{FS}	$V_{DS}=15\text{V}, I_D=3.0\text{A}$		8.5		S
DYNAMIC PARAMETERS (Note1)						
Input Capacitance	C_{ISS}	$V_{GS}=0\text{V}, V_{DS}=25\text{V}, f=1.0\text{MHz}$		320		pF
Output Capacitance	C_{OSS}			80		pF
Reverse Transfer Capacitance	C_{RSS}			17		pF
SWITCHING PARAMETERS						
Total Gate Charge (Note 3)	Q_G	$V_{DS}=50\text{V}, V_{GS}=10\text{V}, I_D=1.3\text{A}$ $I_G=100\mu\text{A}$		27	75	nC
Gate to Source Charge (Note 3)	Q_{GS}			2.4		nC
Gate to Drain Charge (Note 3)	Q_{GD}			6.8		nC
Turn-ON Delay Time (Note3)	$t_{D(\text{ON})}$	$V_{DD}=30\text{V}, R_L=7.5\Omega, I_D=0.5\text{A},$ $V_{GEN}=10\text{V}, R_G=25 \Omega$		28	58	ns
Rise Time (Note 3)	t_R			30	60	ns
Turn-OFF Delay Time (Note 3)	$t_{D(\text{OFF})}$			148	178	ns
Fall-Time (Note 3)	t_F			52	82	ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_c=25^\circ\text{C}$)						
Maximum Pulsed Drain-Source Diode Forward Current	I_{SM}				8.0	A
Drain-Source Diode Forward Voltage (Note 2)	V_{SD}	$I_F=6.5\text{A}, V_{GS}=0\text{V}$		0.9	1.3	V
Reverse Recovery Time	t_{rr}	$I_F=6.5\text{A}, di/dt=100\text{A}/\mu\text{s}$		35	60	ns

Notes: 1. Guaranteed by design, not subject to production testing.

2. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.

3. Independent of operating temperature.

■ TYPICAL CHARACTERISTICS



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