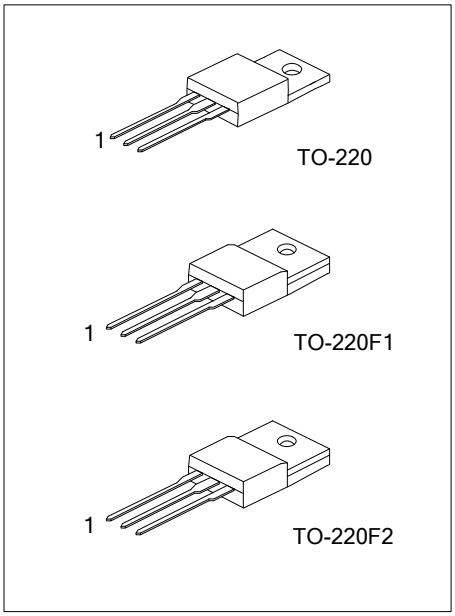
7.0A, 500V N-CHANNEL POWER MOSFET



■ DESCRIPTION

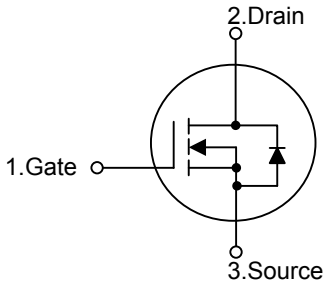
The UTC **7N50** is an N-channel mode power MOSFET using UTC's advanced technology to provide customers with planar stripe and DMOS technology. This technology allows a minimum on-state resistance and superior switching performance. It also can withstand high energy pulse in the avalanche and commutation mode.

The UTC **7N50** is generally applied in high efficiency switch mode power supplies, active power factor correction and electronic lamp ballasts based on half bridge topology.

■ FEATURES

* $R_{DS(ON)}$ < 1.0Ω @ V_{GS}=10V, I_D=3.5A
* High Switching Speed
* 100% Avalanche Tested

■ SYMBOL



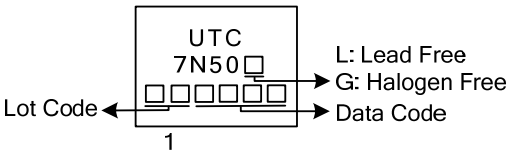
■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
7N50L-TA3-T	7N50G-TA3-T	TO-220	G	D	S	Tube
7N50L-TF1-T	7N50G-TF1-T	TO-220F1	G	D	S	Tube
7N50L-TF2-T	7N50G-TF2-T	TO-220F2	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

7N50L-TA3-T (1)Packing Type (2)Package Type (3)Green Package	(1) T: Tube (2) TA3: TO-220, TF1: TO-220F1, TF2: TO-220F2 (3) L: Lead Free, G: Halogen Free and Lead Free

■ MARKING



■ ABSOLUTE MAXIMUM RATINGS (T_C=25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	500	V
Gate-Source Voltage		V_{GSS}	±30	V
Drain Current	Continuous (T_C=25°C)	I_D	7 (Note 5)	A
	Pulsed (Note 2)	I_{DM}	28 (Note 5)	A
Avalanche Current (Note 2)		I_{AR}	7	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	270	mJ
	Repetitive (Note 4)	E_{AR}	8.9	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	4.5	V/ns
Power Dissipation (T_C=25°C)	TO-220	P_D	142	W
	TO-220F1		48	W
	TO-220F2		50	W
Junction Temperature		T_J	+150	°C
Storage Temperature		T_{STG}	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Repetitive Rating: Pulse width limited by maximum junction temperature
3. L = 10mH, I_{AS} = 7A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C
4. I_{SD} ≤ 7A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C

■ THERMAL DATA

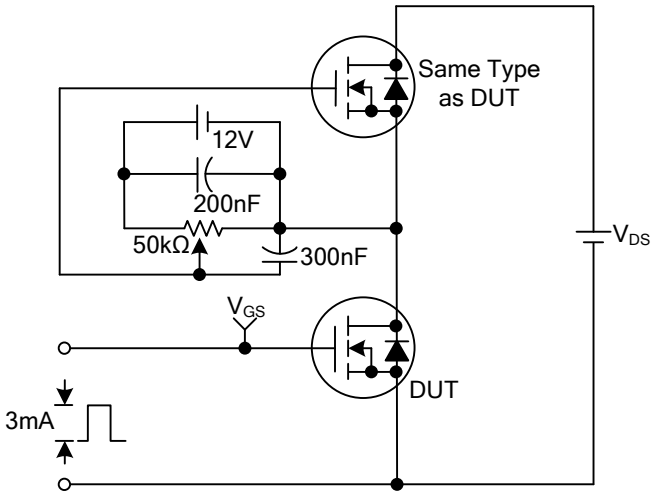
PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient		θ_{JA}	62.5	°C/W
Junction to Case	TO-220	θ_{JC}	0.88	°C/W
	TO-220F1		2.6	°C/W
	TO-220F2		2.5	°C/W

■ ELECTRICAL CHARACTERISTICS (T_C=25°C, unless otherwise noted)

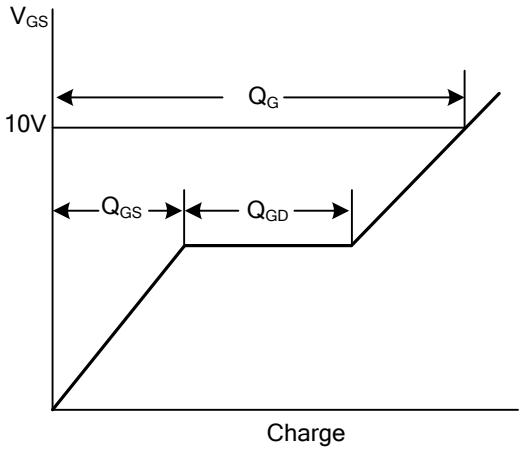
PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV_{DSS}	I_D=250μA, V_{GS}=0V	500			V
Drain-Source Leakage Current		I_{DSS}	V_{DS}=500V, V_{GS}=0V			1	μA
			V_{DS}=400V, T_C=125°C			10	
Gate- Source Leakage Current	Forward	I_{GSS}	V_{GS}=+30V, V_{DS}=0V			+100	nA
	Reverse		V_{GS}=-30V, V_{DS}=0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=250μA	3.0		5.0	V
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	V_{GS}=10V, I_D=3.5A		0.8	1.0	Ω
DYNAMIC PARAMETERS							
Input Capacitance		C_{ISS}	V_{GS}=0V, V_{DS}=25V, f=1.0MHz		720	940	pF
Output Capacitance		C_{OSS}			95	190	pF
Reverse Transfer Capacitance		C_{RSS}			9	13.5	pF
SWITCHING PARAMETERS							
Total Gate Charge		Q_G	V_{GS}=10V, V_{DS}=400V, I_D=7A (Note 1, 2)		12.8	16.6	nC
Gate to Source Charge		Q_{GS}			3.7		nC
Gate to Drain Charge		Q_{GD}			5.8		nC
Turn-ON Delay Time		$t_{D(ON)}$	V_{DD}=250V, I_D=7A, R_G=25Ω (Note 1, 2)		6	20	ns
Rise Time		t_R			55	120	ns
Turn-OFF Delay Time		$t_{D(OFF)}$			25	60	ns
Fall-Time		t_F			35	80	ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I_S				7	A
Maximum Body-Diode Pulsed Current		I_{SM}				28	A
Drain-Source Diode Forward Voltage		V_{SD}	I_S=7A, V_{GS}=0V			1.4	V
Body Diode Reverse Recovery Time		t_{rr}	I_S=7A, V_{GS}=0V, dI_F/dt=100A/μs (Note 1)		275		ns
Body Diode Reverse Recovery Charge		Q_{RR}			0.04		μC

Notes: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%.
2. Essentially independent of operating temperature.

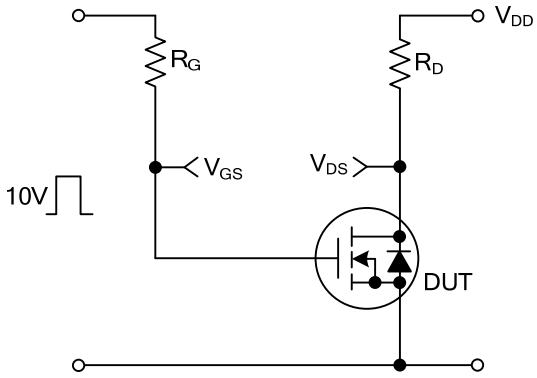
■ TEST CIRCUITS AND WAVEFORMS



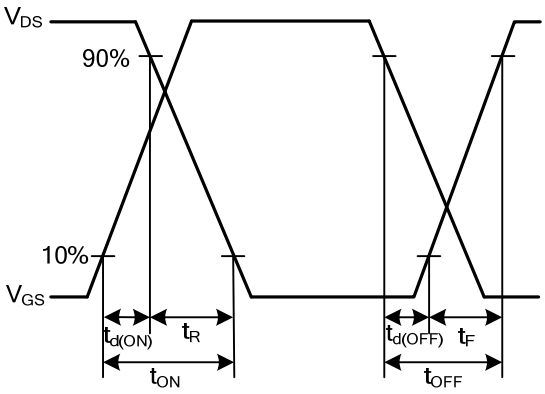
Gate Charge Test Circuit



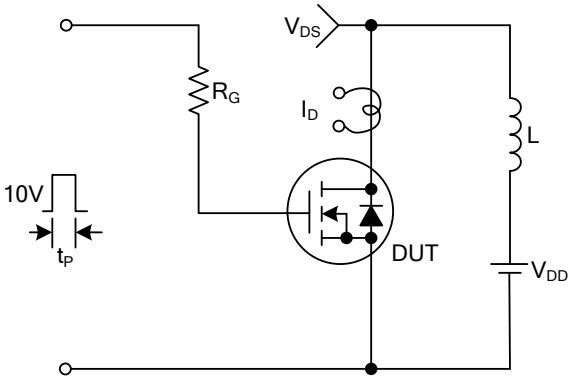
Gate Charge Waveforms



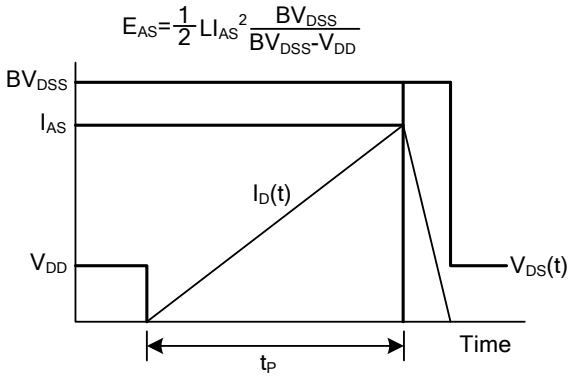
Resistive Switching Test Circuit



Resistive Switching Waveforms

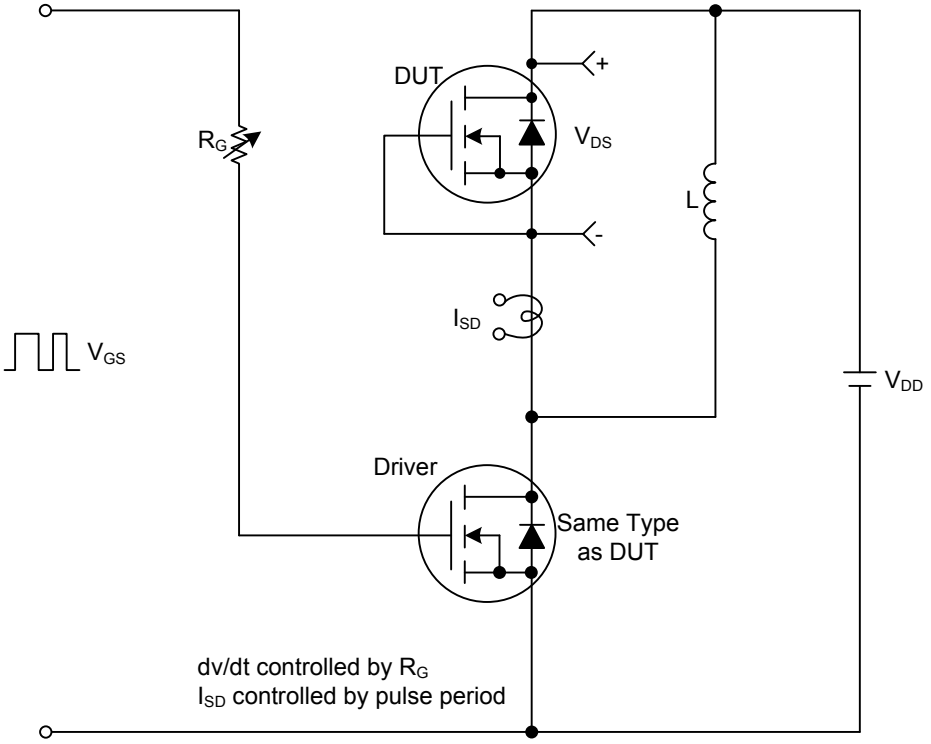


Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

■ TEST CIRCUITS AND WAVEFORMS(Cont.)



Peak Diode Recovery dv/dt Test Circuit & Waveforms