



# U74LVC2G34

**CMOS IC**

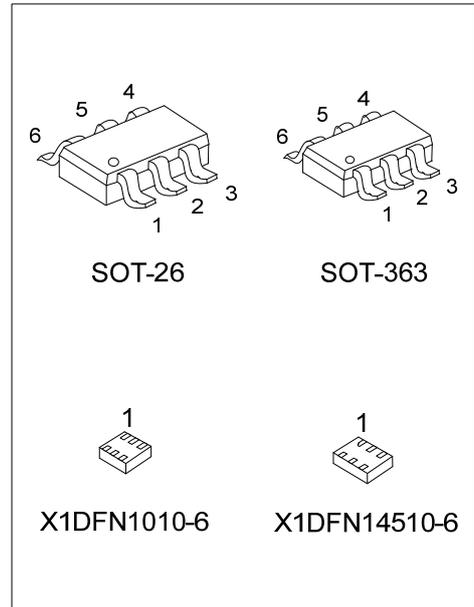
## DUAL BUFFER GATE

### DESCRIPTION

The **U74LVC2G34** is a dual buffer, it provides the function  $Y = A$ .  
 This device has power-down protective circuit, preventing device destruction when it is powered down.

### FEATURES

- \* Operate From 1.65V to 5.5V
- \* Inputs Accept Voltages to 5.5V
- \* I<sub>OFF</sub> Supports Partial-Power-Down Mode
- \* Low Power Dissipation
- \* Max t<sub>PD</sub> of 4.1 ns at 3.3V



### ORDERING INFORMATION

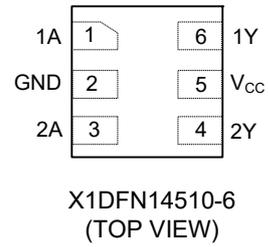
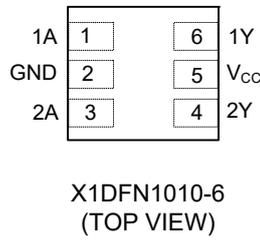
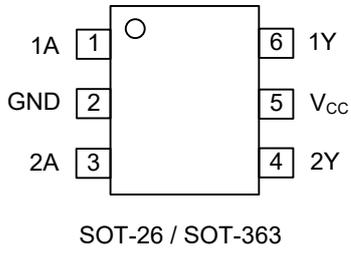
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74LVC2G34L-AG6-R	U74LVC2G34G-AG6-R	SOT-26	Tape Reel
U74LVC2G34L-AL6-R	U74LVC2G34G-AL6-R	SOT-363	Tape Reel
U74LVC2G34L-K06-1010X1-R	U74LVC2G34G-K06-1010X1-R	X1DFN1010-6	Tape Reel
U74LVC2G34L-KAP-R	U74LVC2G34G-KAP-R	X1DFN14510-6	Tape Reel

<p>U74LVC2G34G-AG6-R</p> <p>(1) Packing Type                  (2) Package Type                  (3) Green Package</p>	<p>(1) R: Tape Reel                  (2) AG6: SOT-26, AL6: SOT-363,                  K06-1010X1: X1DFN1010-6, KAP: X1DFN14510-6                  (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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### MARKING

SOT-26 / SOT-363	X1DFN1010-6	X1DFN14510-6
<p>L: Lead Free                  G: Halogen Free</p>		<p>L: Lead Free                  G: Halogen Free</p>

■ PIN CONFIGURATION

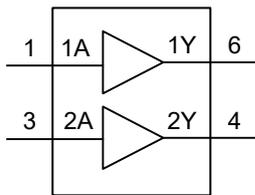


■ FUNCTION TABLE

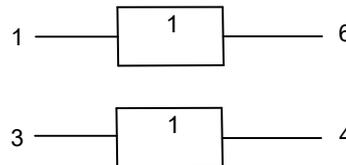
INPUT(nA)	OUTPUT(nY)
H	H
L	L

Note: H: HIGH voltage level; L: LOW voltage level.

■ LOGIC DIAGRAM (Positive Logic)



Logic Symbol



IEC Logic Symbol

## ■ ABSOLUTE MAXIMUM RATING

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage		$V_{CC}$	-0.5 ~ +6.5	V
Input Voltage		$V_{IN}$	-0.5 ~ +6.5	V
Output Voltage	Active mode	$V_{OUT}$	-0.5 ~ $V_{CC}+0.5$	V
	Power-down mode		-0.5 ~ +6.5	V
$V_{CC}$ or GND Current		$I_{CC}$	±100	mA
Continuous Output Current ( $V_{OUT}=0$ to $V_{CC}$ )		$I_{OUT}$	±50	mA
Input Clamp Current ( $V_{IN}<0$ )		$I_{IK}$	-50	mA
Output Clamp Current ( $V_{OUT}<0$ or $V_{OUT}>V_{CC}$ )		$I_{OK}$	-50	mA
Power Dissipation ( $T_A=-40^{\circ}C$ to $+125^{\circ}C$ )	SOT-26	$P_D$	360	mW
	SOT-363		300	mW
	X1DFN1010-6		200	mW
	X1DFN14510-6			mW
Storage Temperature Range		$T_{STG}$	-65 ~ +150	$^{\circ}C$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

## ■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	$V_{CC}$	Operating	1.65		5.5	V
Input Voltage	$V_{IN}$		0		5.5	V
Output Voltage	$V_{OUT}$	Active mode	0		$V_{CC}$	V
		$V_{CC}=0V$ , Power-down mode	0		5.5	V
Input Rise or Fall Times	$t_R / t_F$	$V_{CC}=1.65V \sim 2.7V$	0		20	ns/V
		$V_{CC}=2.7V \sim 5.5V$	0		10	ns/V
Operating Temperature	$T_A$		-40		+125	$^{\circ}C$

## ■ ELECTRICAL CHARACTERISTICS ( $T_A=25^{\circ}C$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Input Voltage	$V_{IH}$	$V_{CC}=1.65V \sim 1.95V$	$0.65 \times V_{CC}$			V
		$V_{CC}=2.3V \sim 2.7V$	1.7			V
		$V_{CC}=3V \sim 3.6V$	2			V
		$V_{CC}=4.5V \sim 5.5V$	$0.7 \times V_{CC}$			V
Low-Level Input Voltage	$V_{IL}$	$V_{CC}=1.65V \sim 1.95V$			$0.35 \times V_{CC}$	V
		$V_{CC}=2.3V \sim 2.7V$			0.7	V
		$V_{CC}=3V \sim 3.6V$			0.8	V
		$V_{CC}=4.5V \sim 5.5V$			$0.3 \times V_{CC}$	V
High-Level Output Voltage	$V_{OH}$	$V_{CC}=1.65 \sim 5.5V, I_{OH}=-100\mu A$	$V_{CC}-0.1$			V
		$V_{CC}=1.65V, I_{OH}=-4mA$	1.2			V
		$V_{CC}=2.3V, I_{OH}=-8mA$	1.9			V
		$V_{CC}=2.7V, I_{OH}=-12mA$	2.2			V
		$V_{CC}=3.0V, I_{OH}=-24mA$	2.3			V
		$V_{CC}=4.5V, I_{OH}=-32mA$	3.8			V
Low-Level Output Voltage	$V_{OL}$	$V_{CC}=1.65 \sim 5.5V, I_{OL}=100\mu A$			0.1	V
		$V_{CC}=1.65V, I_{OL}=4mA$			0.45	V
		$V_{CC}=2.3V, I_{OL}=8mA$			0.3	V
		$V_{CC}=2.7V, I_{OL}=12mA$			0.4	V
		$V_{CC}=3.0V, I_{OL}=24mA$			0.55	V
		$V_{CC}=4.5V, I_{OL}=32mA$			0.55	V

■ ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Leakage Current	$I_{I(LEAK)}$	$V_{IN}=5.5V$ or GND, $V_{CC}=5.5V$			± 5	μA
Power OFF Leakage Current	$I_{OFF}$	$V_{IN}$ or $V_{OUT}=5.5V$ , $V_{CC}=0V$			±10	μA
Quiescent Supply Current	$I_Q$	$V_{IN}=5.5V$ or GND, $I_{OUT}=0$ $V_{CC}=5.5V$			10	μA
Additional Quiescent Supply Current Per Input Pin	$\Delta I_Q$	$V_{CC}=2.3 \sim 5.5V$ , $I_{OUT}=0$ One input at $V_{CC}-0.6V$ , Other inputs at $V_{CC}$ or GND			500	μA
Input Capacitance	$C_{IN}$			2.5		pF

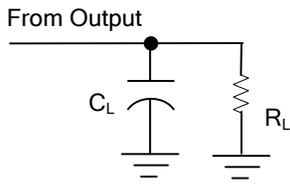
■ SWITCHING CHARACTERISTICS ( $T_A=25^\circ C$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Propagation delay from input (nA) to output(nY)	$t_{PLH} / t_{PHL}$	$C_L=30pF$	$V_{CC}=1.65V \sim 1.95V$ , $R_L=1K\Omega$	1.0	3.8	8.6	ns
			$V_{CC}=2.3V \sim 2.7V$ , $R_L=500\Omega$	0.5	2.4	4.4	ns
		$C_L=50pF$	$V_{CC}=2.7V$ , $R_L=500\Omega$	0.5	2.5	5.0	ns
			$V_{CC}=3.0V \sim 3.6V$ , $R_L=500\Omega$	0.5	2.2	4.1	ns
			$V_{CC}=4.5V \sim 5.5V$ , $R_L=500\Omega$	0.5	1.9	3.2	ns

■ OPERATING CHARACTERISTICS ( $T_A=25^\circ C$ , unless otherwise specified)

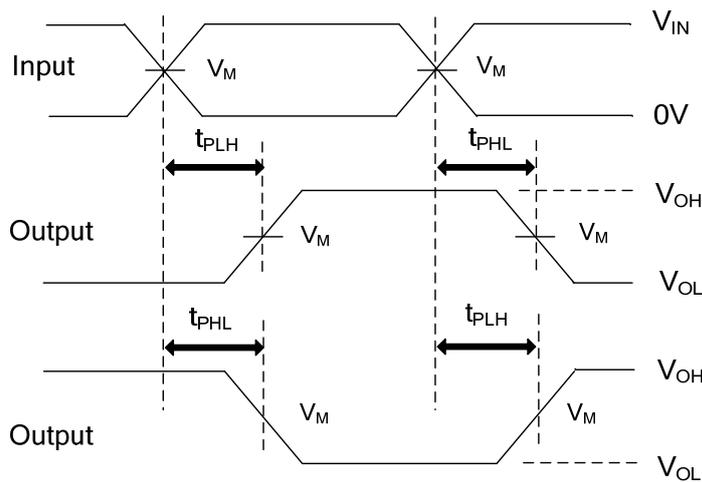
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	$C_{PD}$	$V_{CC}=3.3V$ , $V_{IN}=GND$ to $V_{CC}$		20		pF

■ TEST CIRCUIT AND WAVEFORMS



TEST CIRCUIT

$V_{CC}$	INPUTS		$V_M$	$C_L$	$R_L$
	$V_{IN}$	$t_R, t_F$			
1.65V ~ 1.95V	$V_{CC}$	$\leq 2\text{ns}$	$V_{CC}/2$	30pF	1K $\Omega$
2.3V ~ 2.7V	$V_{CC}$	$\leq 2\text{ns}$	$V_{CC}/2$	30pF	500 $\Omega$
2.7V	2.7V	$\leq 2.5\text{ns}$	1.5V	50pF	500 $\Omega$
3.0V ~ 3.6V	2.7V	$\leq 2.5\text{ns}$	1.5V	50pF	500 $\Omega$
4.5V ~ 5.5V	$V_{CC}$	$\leq 2.5\text{ns}$	$V_{CC}/2$	50pF	500 $\Omega$



PROPAGATION DELAY TIMES

Note:  $C_L$  includes probe and jig capacitance.

All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10\text{MHz}$ ,  $Z_o = 50\Omega$ .

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